TestWay

The reference in Design for Excellence (DfX)

Press Release:

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ASTER Technologies, the leading supplier in Board-Level Testability and Test Coverage analysis products, has developed a major new release of **TestWay,** the reference in **Design for Excellence (DfX)**, by incorporating an integrated workflow from design through to product delivery.

DfX also referred to "Design for Money" can be used as part of an organization's Continuous Improvement Programme to decrease product development time, product cost and manufacturing cycle time, while increasing product quality, reliability and ultimately the customer satisfaction.
It will significantly decrease the overall cycle time from the design concept to customer delivery, which is a critical success factor.
Design for Excellence makes it possible to implement a Lean Test approach that produces a lower cost product whilst maintaining the highest quality.

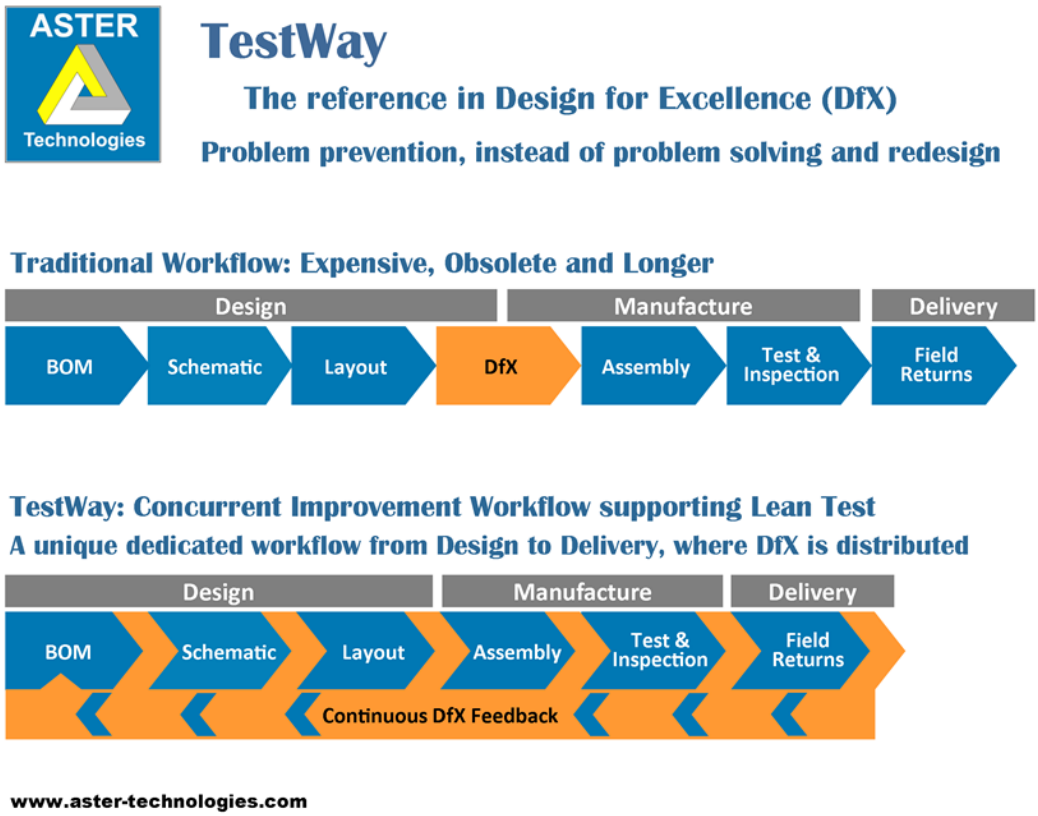
ASTER's vision is articulated on two principles: ❶ Using traceability and repair loop information in order to qualify the customer defect universe. The defects include design defects, manufacturing defects and functional defects. ❷ Using **TestWay** to import the defect opportunities and identify the possible consequences of inadequate testability and test coverage on a new design.

Traditionally, manufacturing and test constraints are only considered at the end of the layout phase, prior to transfer of the CAD data to production. Due to board complexity, it is now mandatory to consider a validation stage at each step of the design and manufacturing phases. **TestWay** has been developed to allow users to analyze each stage of the design to delivery workflow.

This is achieved by the following stages:

- **Design for Component** – When the key components are selected, **TestWay** checks ROHS, reliability, DPMO, BSDL file validation in order to guide component selection.
- **Electrical Design for Test** – When the schematic sheets are defined, **TestWay** verifies electrical DfT guide lines. It includes standard checks and customer's specific checks relating to specific company requirements. By simulating the test strategy prior to the layout phase, helps to minimize the need for physical accesses in alignment with the defect universe. It helps to reduce test point access by 30% to 70%!
- **Mechanical Design for Test** – When the layout is finalized, **TestWay** optimizes test probe placement according to test strategy definitions, estimates the test coverage, models the cost and calculates the production yield and TL9000 initial return rates.
- **Design to Build and Design to Test**, **TestWay** estimates test coverage using theoretical models for a wide range of test and inspection strategies. These include APM (Automated Placement Machines), AOI, AXI, BST (Boundary-scan Test), FPT (Flying-probe Test), ICT and Functional Test. These models can be tuned to reflect the test and measurement capabilities of each individual target tester. **TestWay** exports the CAD data into the native format useable by Assembly machines, Automated Optical Inspection, Automated X-Ray, In-Circuit testers, Flying –Probe testers and Boundary-Scan testers in alignment with the simulated strategy. The outputs include the assembly and test programs, or input lists and test models, as well as test fixture files.

- **Test for Excellence** –Once the test/inspection programs have been debugged and released, **TestWay** can read the completed test program or test report and compare the coverage between the estimated and measured analysis. The resultant analysis reports define the test coverage using industry standard metrics that enable the user to identify any misalignment between the estimated and real coverage.
  Quality traceability tools used in the diagnosis and repair of printed circuit boards can take advantage of detailed test coverage analysis to improve the diagnostic resolution and speed up the repair process.
- **Test for Designability** – Test is an important contributor for design improvement, as soon as a feedback loop between production and design has been organized.



CAD importers supporting schematic netlist, layout, schematic graphics and design or test models are available for the wide range of EDA tools used within the industry today. This is a key differentiator from other commercial DfX tools that work only from the layout stage, which is often too late in the design process to be of use. TestWay operates directly from native CAD formats, ensuring the full interoperability between all stages across the design-manufacturing flow.

With **TestWay**, all these stages are managed within a single tool using an integrated methodology.

About ASTER Technologies
ASTER is the leading supplier in Board-Level Testability analysis tools, capitalizing on proven expertise in board testability and strong customer relations. Founded in 1993, ASTER develops a wide range of products dealing with PCB Testability, Viewing and Quality Management. TestWay is a proven solution, used by many PCB design and manufacturing companies worldwide that provides a unique approach to identify electrical testability requirements and compute theoretical test coverage early in the design chain.

For more information, or to get a demonstration of these new features, why not visit ASTER Technologies at Booth **1E52** during the NEPCON-China show in Shanghai between 23rd and 25th April, 2013. Alternatively visit www.aster-technologies.com or call +33 299 830101.