# JTAG-centric board testing demands EARLY DESIGN INPUT

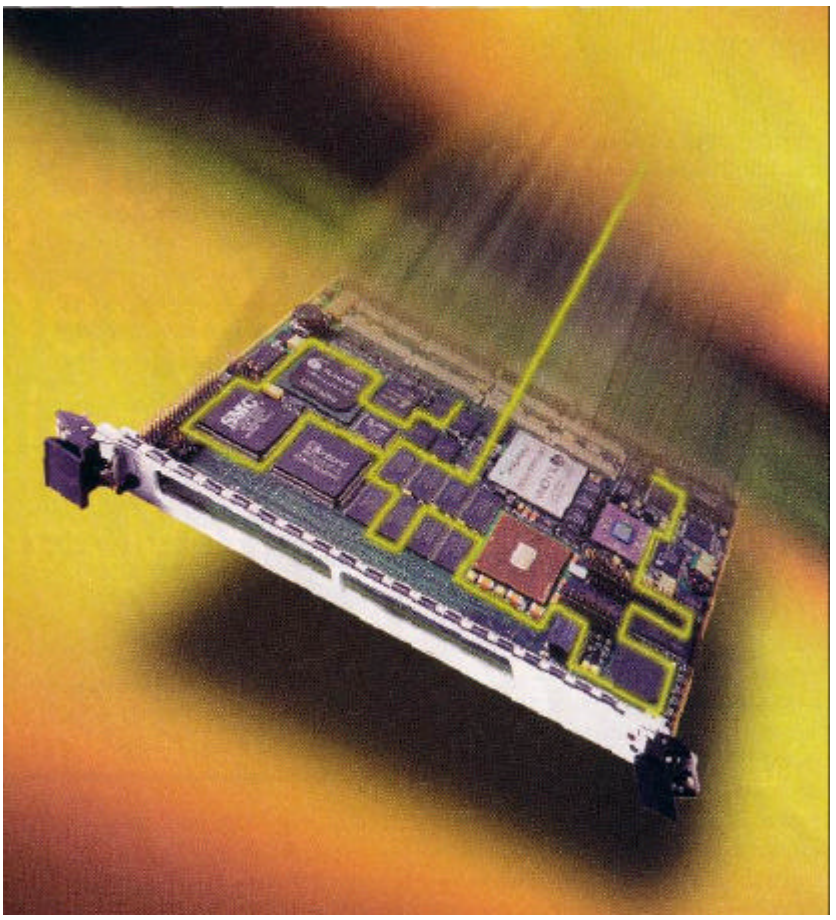
OVER THE YEARS, engineers have used the metaphor "throwing projects over the wall" to describe the practice in which one department in a product-design chain completes the fundamentals of its part of the design, then hands it off to the next group. It implies that the handover occurs with scant regard for the impact that decisions

made by the first group have on the work of the second group. Throwing projects over the wall is, therefore, invariably regarded as poor practice, yet it still goes on. One such transition is from the completed layout of a circuit board to subsequent process steps, to test development, and to production. The industry has promoted the desirability of a coherent DFT (design-for-test) strategy over many years, often with the aid of presentation slides showing cartoons that depict dividing walls between departments.

**AS BOUNDARY-SCAN TESTING BECOMES THE DOMINANT METHOD FOR FINDING MANUFACTURING DEFECTS, DESIGN-FOR-TEST DECISIONS INCORPORATED AT BOARD DESIGN AND LAYOUT MUST TAKE ACCOUNT OF ALL OF THE DOWNSTREAM TEST PROCESSES.**

## DENSITY DRIVES OUT PADS

Now, trends in component and board design are dictating the pace of enforcing a consistent DFT policy. Fine-pitch BGA packages are becoming much more commonplace and are, increasingly, the only package option available for many functions. This trend goes hand-in-hand with the packages' increased functional complexity. To route a board containing even one such device challenges the more modest pc-board layout packages. Placing several high-density packages on a pc board requires the full palette of deep multilayer boards, fine-track-and-gap geometries, and buried vias. A 32-bit microcontroller has 300 to 400 I/Os on a BGA package with, typically, 1.27-mm ball spacing. If you choose to use the more complex programmable devices-contained in some of the most I/0-intensive packages on the market today-the pin count can escalate even further. The most complex device in Altera's Apex-II family, for example, has 1508 I/Os on a fine-pitch (1-mm) BGA package. Xilinx manages to top that by a few; the flagship of its Virtex-II series sports no fewer than 1517 ball terminations.



Boards that use devices of this class place heavy demands on assembly technology and must be comprehensively tested for manufacturing integrity. You cannot rely on physical test access and probing; many signals are routed entirely on internal layers within the board and are unavailable for test access without intervention. You may have components mounted on the underside of the board. Even if you do not, the track density will be high, and you will have limited opportunities to bring signals to the board surface for physical access. Further, even if you find the space on the surface, you need to find space on all the layers between the most accessible point of signal routing and the surface, to place the necessary vias. Even if you succeed, there is a cost associated with adding tracking that is additional to the extra design effort; more vias means more bare-board manufacturing complexity and a potential reliability penalty, even if it is a small one. If you are designing boards with that class of high-density components, you will likely be concerned with delay times for signal propagation across the board. Therefore, unnecessarily loading tracks becomes undesirable.

Hence, the panoply of test methods that can be brought to bear on the assembled board, in addition to the traditional in-circuit test techniques, includes automatic optical inspection, X-ray inspection, and boundary scan, also known as JTAG, IEEE-1149.1. References **1** and **2** describe how although the progress of boundary scan has been a "slow burn," it is now a major component of the suite of available manufacturing-test options.

## EXPLORING TRADE-OFFS

One problem at the design stage is evaluating the trade-offs involved in preparing for downstream test processes. Once you have established a design's functionality and component selection and board layout is underway, a range of choices presents itself. How much effort does seeking out component variants that have boundary scan justify, as opposed to using variants that do not? What level of test coverage is available from a given set of components and a given layout? What is the minimum set of changes necessary to raise that figure to a specified acceptable level? What degree of coverage can you obtain from automated optical or X-ray testing, and to what extent can this coverage offset the need to add coverage by in-circuit or boundary-scan testing? If you can find enough space for an appreciable number of conventional test pads, will you use them with a conventional bed-of-nails test fixture or with a flying-probe tester, in which moving probes visit the pads, in turn, testing sequentially rather than in parallel? (If so, the economics of testing time become a greater part of the overall equation, and again, you must trade off the number of test points against the test coverage that other methods achieve.) These questions are the domain of "testability analysis," a discipline that is fast becoming necessary to carry out in parallel with board design and layout.

The necessary constraints apply beyond the handover of a board from layout to testing. The early days of scan based testing-around 20 years ago-placed considerable emphasis on access to complete systems as a maintenance and diagnostic aid (see **sidebar** "Extending to system level"). Now, that vision is being realised, but it implies that virtually every group with an interest in any stage of a product's life cycle-from component purchasing through field service-has an interest in the definition of the test strategy and test-access arrangements. This situation reveals a key fact about DFT for complex products: It is not only a technology issue but an organisational and methodology problem, as well.

Getting DFT right means soliciting the input of every engineer who interacts with the product throughout its life,

not just the test developer who is next in line. And it means getting those inputs early enough to make them part of the first pass of the board layout, not a retrofit or an afterthought. DFT consultant Ben Bennetts of Bennetts Associates cites a simple example: If a field-service engineer has JTAG access to the board, the standard already contains a provision for board and device identity and for revision data to be read out. However, he notes, this provision is an option, not a requirement, and you would only include it if the designer has sought the field-service engineer's input on what he or she would find useful. This same principle lies at the heart of the structure outlined in the **sidebar** "Boundary scan takes centre stage." Bennetts notes that the conventional approach to the problem, grounded in in-circuit testing, is to analyse the schematic, determine what nets you need to access for testing, then subtract from that list any nets that boundary scan testing can reach. Now that boundary-scan-centric test regimes are becoming more common, a new approach is necessary.

Given all these inputs, how do you assess them and shape a workable strategy?

### AT A GLANCE

- Escalating device complexity and interconnection density is increasing demands on manufacturing testing.
- Bringing all signals to the surface of the circuit board for probing is no longer feasible.
- JTAG-based test strategies underpin a blend of test techniques; software tools can assist.
- DFT for complex products is much about methodology and organisation as it is about technology.
- Test strategy must consider all stages of the product's life cycle and must be included in the earliest stages of design.

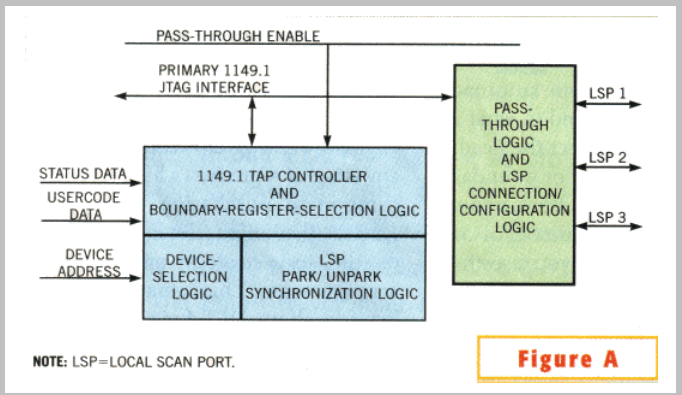
The industry is providing software assistance. TestWay, from independent French company Aster Ingenierie, directly targets this function. Company founder and product manager Christophe Lotz describes TestWay as "a real DFT tool that you can use in both design and test". You can use TestWay early in the design process, to do what-if explorations of the various options. In effect, it acts as a test process simulator that models the consequences of all of the testing options open to you. The result is a series of estimates of fault coverage that reflect the choices you make. You can also use the tool to fully evaluate the testability of a board whose layout is already complete and investigate how you might improve the coverage either by test-process design or by making the minimum changes necessary to add test-access points to the board.

According to Lotz, density and the need to get good coverage without the physical access of the traditional in-circuit type, is primarily driving the trend. TestWay analyses a number of inputs, including the physical layout of the board,

## EXTENDING TO SYSTEM LEVEL

In a complex system comprising multiple complex circuit boards on a backplane, the idea of extending the test facility that a JTAG-based architecture affords to encompass the entire system is attractive. Through a single port, diagnostic data for the complete system is available. To implement this concept, you must route the JTAG data across the backplane. By testing board-to-board interconnections, you implicitly test the interconnections that the backplane provides to the boards it carries. The connection from the backplane to the outside world might be made directly to a local PC-based tester or any other test system. It might also occur through a LAN or WAN connection. The latter connection takes the architecture into the realm of remote system control, diagnostics, and software upgrading, whether by reconfiguring programmable-logic devices through their JTAG ports or by reloading the contents of flash memory.

To enable this structure, you must provide a JTAG interface between each major circuit board and the system backplane. To avoid issues of excessively long and complex scan chains and to separate the task into manageable segments, you need to separately address each of the boards within the system. A number of semiconductor vendors, including Texas Instruments, Lattice Semiconductor and National Semiconductor, have devices that function as bridge chips. Firecron is a fabless semiconductor company that specialises in this area. The company designs its JTS03 and 06 cips to be placed between each board and the backplane, sitting on a common JTAG connection across the backplane (but physically resident on each board). The chips are individually addressable and can place their local scan chains on the backplane or isolate them from it, enabling a multidrop capability, The 03 and 06 designations denote the chips' capability to interface with multiple, smaller scan chains on each circuit board (three or six, respectively). According to Firecron, this partitioning will yield better fault diagnostics, as a fault on one local scan port will not leave the circuit board untestable. It will also achieve faster programming of flash memory via the scan chain and will yield benefits in reduced signal loading. In operation, you can address the device to connect any of its local scan ports into the active scan chain or set the local port to a pass-trough mode that is transparent to the IEEE 1149.1 signals **(Figure A)**.

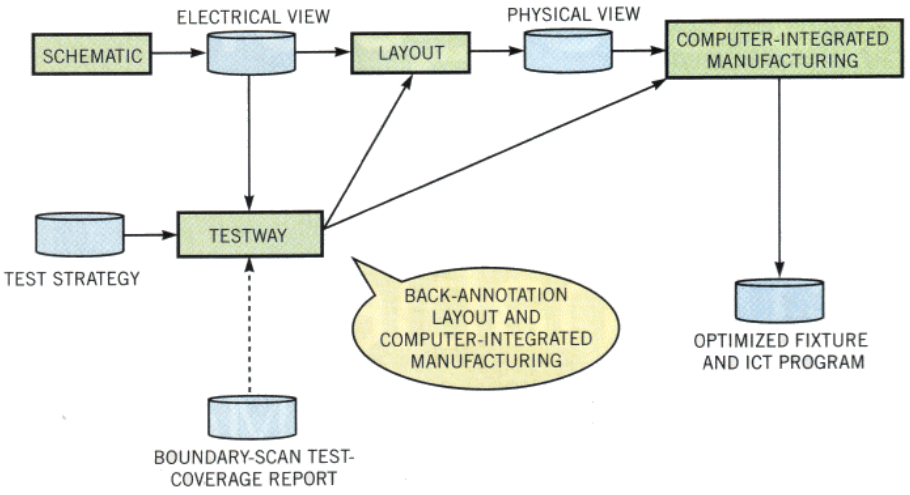



**Firecron's JTS 03 both bridges a board's scan chain to a backplane IEEE1149.1 connection and makes three smaller scan-chain accesses available on the board.**

from pc-board-layout CAD files. It also takes as inputs data on the components, including whether the ICs have boundary-scan-enabled designs. If TestWay finds that the ICs are boundary-scan-enabled, the software also makes use of the ICs' BSDL files. (The BSDL describes the scan chain that each device offers to verify its connectivity.)

You can manipulate the connectivity of the board in the model that the software creates, adding or removing points or nets and adding or removing boundary-scan capabilities. You can also add extra logic for test access, and you can move up the system hierarchy to incorporate board-to-board interconnect into the model. Boundary-scan techniques primarily concern logic components, although as **Reference 1** describes, they are being extended to analogue parts. However, TestWay can accomodate analogue measurements in its test scenarios, as well as a range of other paramters relevant to test process.

Lotz describes the way in which you can combine tests to build confidence in the manufacturing of the board. If you have used, say, optical and X-ray inspection to verify that all of the solder joints appear to have been completed correctly and you have boundary-scan data that confirms that the boundary-scan testable joints have all been properly made, then your confidence that board has been properly manufactured greatly increases. Similarly, you may not have the resources, time, or test access to measure every passive component on the board,




**TestWay uses analysis and back-annotation to produce an optimised boundary-scan program and defines the minimum efficient set of in-circuit access points to achieve coverage of the rest of the board.**

but AOI (automatic optical inspection) can verify that a correctly oriented component has been mounted in each position where one ought to be. Then, if a sample measurement you make on one or a few such components provides a correct value, your confidence that the board assembly has been correctly sequenced, with the correct components, correspondingly increases. The program can calculate the real test coverage of combinations of test techniques, such as boundary-scan-with-in-circuit testing (**Figure 1**), with flying-probe testing, or with cluster testing, for example. (Cluster testing exploits the known signal propagation characteristics of components that do not have boundary-scan capabilities but have a consistent and known I/O response in their tested state. A cluster can be a group of non-JTAG devices with I/Os that you can reach from test-access points.) **Figure 2** shows the way the program classifies circuit nets to determine redundancy in test access.

In assessing the results of combinations of test methods, you can set the software to be "optimistic" or "pessimistic." The optimistic mode of software assumes that, for example, the boundary-scan test will find problems that lie between the scan chain and non boundary-scan nets (in which case, other testing methods will not be required to look for them). The pessimistic mode of software assumes that the test will not find these problems and adds them to a list of faults that other methods will seek.

## BOUNDARY SCAN TAKES CENTRE STAGE

At Motorola's Swindon, UK, site, designing and manufacturing cellular infrastructure systems, internal DFT (design-for-test) consultant Steve Harrison describes a DFT strategy that is minimising in-circuit testing of complex boards for third-generation cellular systems. In some cases, Harrison expects to be able to completely eliminate it. He outlines a tightly structured DFT strategy that relies heavily on boundary-scan testing, His department places boundary-scan-enabled silicon high on preferred component lists and makes compliance with IEEE1149.1 a condition that suppliers to the company must meet. Early project reviews identify non-JTAG parts and specify JTAG alternatives where possible.

Harrison notes that it is not unknown for components to claim to be compliant when, in reality, they aren't. He has encountered disparities as basic as BSDL files that do not match the silicon supplied. Therefore, he demands that suppliers verify and check the syntax of their components' BSDL files.

Qualified parts underpin a DFT strategy that runs throughout the design cycle, with reviews at the schematic stage, at board placement, and following board routing. All interested parties attend the reviews, each representing a stage of the product's testing. Harrison uses TestVVay in its early, predictive, mode to forecast test coverage as the board design evolves. But, he adds, there is still a place for sitting down with a printout of the complete schematic.

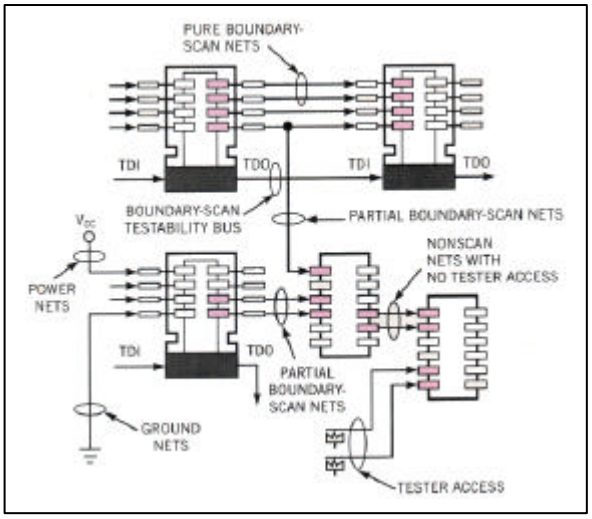
Motorola's intranet site maintains a full set of design guidelines. The test flow, following AOI (automatic optical inspection) and X-ray of soldered joints, maximises use of JTAG and, according to Harrison, "pushes it as far along the design chain as possible."

Many of Motorola's boards use multiple complex ASICs. For these, Motorola uses the LogicVision BIST method, invoking it, where possible, from the JTAG test process.

Lotz envisions that TestWay will eventually link to more and more data from other domains mechanical information from component and board libraries to optimise the contribution of Xray and AOI tests, for example-allowing the user to remove redundant tests. As in other areas of design, data reuse is key.

Each of the main manufacturers of manufacturing-test equipment has its own software offerings to help you optimise a test strategy. Agilent, one of the key players in the traditional in-circuit test arena with its 3070 system (and also a provider of AOI and X-ray inspection), has recently formed an alliance with Asset InterTech, provider of PC driven JTAG testing and in-system programming tools. Under the agreement, Agilent will integrate Asset's ScanWorks boundary-scan system into the 3070 tester to provide combined test capabilities that will reuse boundary-scan tests developed in designing and debugging throughout the product's testing cycle. According to Kevin Jones, Agilent's Northern European business manager for electronic test products, the test data will be reused in the 3070, and again in field testers. The tool suite will offer support for checking whether a circuit-board layout's test points are missing. If they are missing, the software will determine whether access is still possible via clustering. Jones sees the same need for a tool chain that passes and reuses data through a number of test processes, eliminating duplication of effort and redundant testing.

Part of JTAG Technologies' software tool chain, the Boundary Scan Examiner, assesses boundary-scan coverage once you've created a first layout of the board. It computes a net-by-net percentage coverage that you achieve using scan




**TestWay Interconnect analyser classifies nets into nine categories: ground nets, power nets, unused pins, pins connected only to a pull-up resistor, a boundary-scan testable bus, pure boundary-scan nets, partial boundary scan nets, tester access, and nonscan nets with no tester access.**

mat. You can input the results into the Visualiser package, which presents the same information in graphical form, referring the data back to schematics or to board layout. According to JTAG's UK sales manager James Stanbridge, this facility can provide a useful, quick guide to the efficacy of the test regime. If the density of the indicated fault coverage coincides with the maximum density of pins on the board layout, you are achieving coverage where it is most necessary. JTAG offers a number of other tools for scan-chain based test generation, such as a memory- cluster test generator. To incorporate devices that are not boundary-scan-capable, you must study the data sheets of devices that have all or most of their pins accessible from boundary-scan parts. Analysing their I/0 responses to given signals propagated from the adjacent boundary-scan devices' pins allows you to test their connectivity along with the scan- chain parts. Stanbridge notes that the nature of boundary-scan testing works in your favour here; complex parts are likely to be too complex to analyse in this way, but the likelihood is that the most complex parts on your board will be the scan-enabled ones, and nonscan parts will be the simpler ones.

Test-equipment supplier Goepel also has a software offering that automatically prepares testbenches from data input in BSDL. However, it again focuses on test preparation for a given layout and is intended to be used once such a layout is available. Goepel will support explorations of design options at an earlier phase of your design through an agreement with Aster Ingenierie. ■

You can reach Editor Graham Prophet at +44 118 935 1650, fax +44 118 935 1670 e-mail graham.prophet@cahnerseurope.com.

## FOR MORE INFORMATION…

For more information on products such those discussed in this article, go to www.edn-info.com. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

**Agilent Technologies**
www.agilent.com

**Altera**
www.altera.com

**Asset Intertech**
www.asset-intertech.com

**Aster Ingenierie**
www.aster-ingenierie.com

**Bennets Associates**
www.dft.co.uk

**Firecron UK**
www.firecron.com

**Goepel Electronic**
www.goepel.com

**JTAG technologies**
www.jtag.com

**Lattice Semiconductor**
www.latticesemi.com

**Motorola**
www.mototola.com

**National Semiconductor**
www.national.com

**Teradyne**
www.teradyne.com

**Texas Instruments**
www.ti.com

**Xilinx**
www.xilinx.com

REFERENCES

1. Marsh, David, "Simple boundary scan techniques tackle sophisticated systems," *EDN Europe, July 200 1,* pg *24.*
2. Marsh, David, "Auto industry drives embedded boundary-scan debugging," *EDN Europe,* August *200 1,* pg *22.*