ENHANCED MANUFACTURING SERVICES 4.0:
THE DIGITAL SUITE TO SUPPORT INDUSTRY 4.0
FROM ELECTRONIC DESIGN TO DELIVERY
ARTICLE 1 – PHILOSOPHY AND DFT 4.0

Industry 4.0 is a name for the current trend of automation and data exchange in manufacturing technologies. Industry 4.0 promotes what has been named "smart factory". Within the modular structured smart factories, cyber-physical systems monitor physical processes, create a virtual copy of the physical world and make decentralized decisions.

There are key principles in Industry 4.0.

- Interoperability: Connect machines, devices, sensors and people to communicate with each other.
- Digital Simulation: Create a virtual copy of the physical world. Play with "What-if" scenarios in the virtual word in order to identify the optimized physical flow. Use theoretical results to control the physical world.
- Convert data into information: Aggregate raw data from cyber-physical systems to build and visualize comprehensive information that allow humans to make decisions based on facts.
- Decentralized decisions: the ability of cyber physical systems to make decisions on their own and to perform their tasks as autonomously as possible.

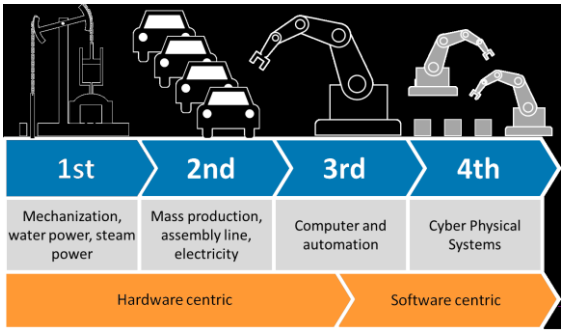

Fig 1: Industry 4.0 - 4th revolution
Credit to Christoph Roser at AllAboutLean.com,

Despite all the fanfare for Industry 4.0, the truth is that many electronic companies still have only a partial understanding of what it is and how it applies to industry. While it might appear complicated from outside, Industry 4.0 is merely a logical extension of the increasing automation and connectivity that has been part of continuous improvement processes for decades.

In some ways, much of the information already exists within a Design to Delivery flow. But these are isolated islands without opportunities for communication. Breaking the wall between departments is the key target.

In order to deliver Defect Free Products, ASTER is promoting a new vision of Design to Delivery flows, by applying the principles of Industry 4.0 principles. It is named **Enhanced Manufacturing Services 4.0 (EMS 4.0)**.

EMS 4.0 can be used as part of an organization's Continuous Improvement Program, to decrease product development time, production cost and manufacturing cycle-time, while increasing product quality, reliability and ultimately the customer satisfaction.

EMS 4.0 is articulated on two principles:
❶ Qualify the customer defect universe using traceability and repair loops (big data analysis). This universe includes not only manufacturing defects, but also design, and functional defects.
❷ Simulate the manufacturing flow from schematic or layout file in order to identify the possible consequences of inadequate testability and test coverage on a new design.

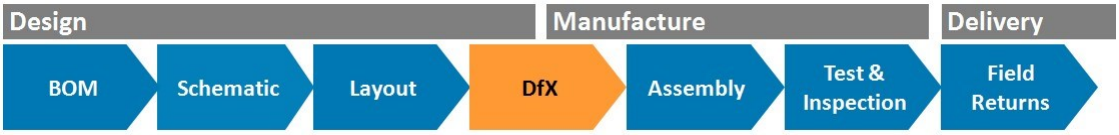

Fig 2: Traditional Workflow: Longer, more expensive and obsolete.

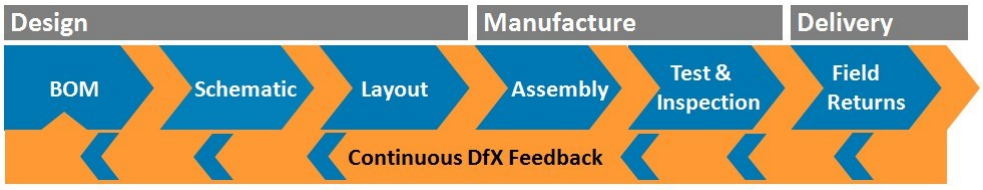

Fig 3: EMS 4.0 Workflow: Improved decision-making, faster time-to-market, cheaper and better quality. Lean design, Test and Manufacturing deliver Defect-Free products at lower cost! ASTER has designed a complete digital software suite including TestWay and QUAD: TestWay flow for Design to Delivery and QUAD traceability for continuous DfX feedback.

Traditionally, manufacturing and test constraints are only considered at the end of the layout phase, just prior to the transfer of CAD data to production. This is too late to have a significant contribution on time to market.

With EMS 4.0, TestWay significantly decreases the overall cycle time from the design concept to customer delivery, which is a critical success factor. It makes it possible to implement a Lean Test approach that produces a lower cost product whilst maintaining the highest quality.

The following stages are addressed:

- **Design for Component** – For key component selection; check the ROHS, reliability, defects per million opportunities (DPMO), and validate boundary-scan description language (BSDL) file, in order to guide component selection.
- **Electrical Design for Test** – Analyze schematic data; verify the testability by conducting electrical rules checking that reflects the Design for Test (DfT) guide lines.
  By simulating the test strategy prior to the layout phase, this helps to minimize the need for physical access necessary to detect defects aligned to the defect universe. It helps to reduce test point requirements by typically 30% to 70%!
- **Mechanical Design for Test** or **Accessibility Analysis** – Often incorrectly referred to as DfT by the industry, but realistically it is only accessibility analysis. Once the layout is finalized, test probe placement should be optimized according to test strategy definitions. The probe access information can then be used for estimating the test coverage, modeling the cost and calculating the production yield and TL9000 initial return rates.
- **Design to Build** and **Design to Test** – Lean test is driven by test coverage estimation using theoretical models reflecting the capabilities of test and inspection strategies, such as:
  - Automated Placement Machines
  - Solder Paste Inspection (SPI)
  - Automatic Optical Inspection (AOI)
  - Automated X-ray Inspection (AXI)
  - Boundary-scan Test (BST)
  - Flying-probe Test (FPT)
  - In-Circuit Test (ICT)
  - Functional Test (FCT)

  These virtual machines can be tuned to reflect the exact test and measurement capabilities of each individual target tester. TestWay simulation is extremely precise and deviation between the virtual and physical worlds is around 1%.

TestWay provides interoperability from native CAD data to any targeted assembly machines, automated optical inspection, automated X-Ray, in-circuit testers, flying-probe testers and boundary-scan testers.

- **Test for Excellence** – Once test and inspection programs have been debugged and released, it is imperative to be able to assess the completed test program or test report and compare the coverage between the estimated and measured analysis. By analyzing the program running on the shop floor, it highlights what is really being tested.

  Industry standard metrics are used in the coverage analysis, in order to make direct comparisons and identify any misalignment between the theoretical and real coverage. Any test escapes can be identified and rectified prior to main stream production.

  Traceability tools used in the diagnosis and repair loops can take advantage of detailed test coverage analysis to **improve the diagnostic resolution** and speed up the repair process.

- **Test for Designability** – Test is an important contributor for design improvement, once continuous DfX feedback between production and design has been established.

EMS 4.0: Design For Test

This first article of three that describes ASTER contributions to the implementation of EMS 4.0 will focus exclusively on Design for Test.

The EMS 4.0 workflow utilizes data analytics to provide continuous assessment at each stage in the Design to Delivery workflow, with feedback provided at each stage.

Companies must deliver good products to their customers; defect free and at minimum cost.

The challenge is how to detect, or prevent defects from occurring, so that only good products are shipped to the customer.

Traditional commercial DfT tools work only from the layout stage, which is too late in the process.

Design data must be analyzed at the earliest stage in the product life cycle by importing schematic data.

Electrical **DfT rules violations** should be identified and rectified prior to commitment for board layout in order to prevent costly design re-spins. These rules can include standard and customer's specific checks, relating to company requirements. With a centralized knowledge database, the same problems will never be repeated!

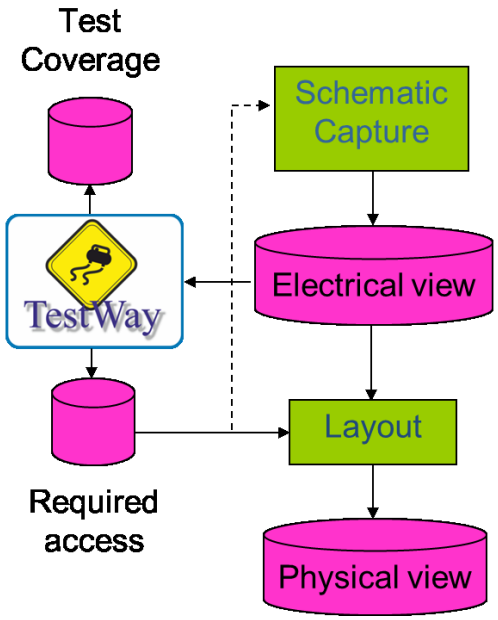

Fig.4 Schematic – Electrical DfT

Test point requirements must also be identified pre-layout, during the schematic capture stage. This reduces the need for unnecessary test access, saving on PCB real estate, particularly on high density boards.

TestWay simulates the test strategy including any combination of inspection and test machines, delivering the **highest**

test coverage. This unique combination provides electrical rules analysis, test point analysis, test strategy optimization and test cost modeling, based purely on schematic information. This, in turn, provides valuable layout guidelines that can be used to optimize the Printed Circuit Board layout.

Once the PCBA layout is completed, a mechanical DfT analysis must be conducted to confirm the nets that require test access are not compromised by solder mask, component outline, adjacent probes constraints etc.

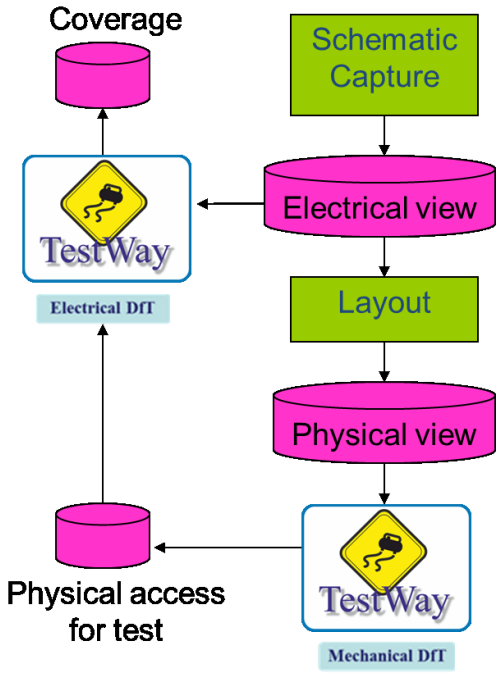

Fig.5 Layout - Mechanical DfT

To be continued

The next article will cover the test coverage definition and how to use it as a key contributor for final product quality. Once the test strategy has been defined, specific test files for each machine in the line can then be generated. These machine files will represent the early simulated test strategy further reducing debug time and redundant testing.

The final article will explain how traceability tools can help improve the design of new products. Quality and yield are directly related to manufacturing processes. Cognitive computing helps manufacturers identify quality issues more efficiently, increase production yield and reduce problems that lead to service and warranty costs.

The EMS 4.0 workflow enables tremendous benefits in time-to-market, cost reduction, quality improvements. Realize your digital transformation now with the ASTER digital suite including TestWay and QUAD.

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