Paradigm Shift – DFT Analysis Driven by Test Coverage Instead of Accessibility

William E. Webb, Jean-Michel Boivin
ASTER Technologies
Colorado, USA
Will.webb@aster-technologies.com

ABSTRACT
Continuing to concentrate on traditional access is not the best way of measuring good test coverage. It can lead to expensive ICT fixtures and lengthy FPT tests which are costly and not necessarily beneficial. This represents a paradigm shift in thinking. Using software tools to calculate the resulting test coverage produced by the access is the key to gaining an understanding of the overall level of test quality. Test coverage analysis of all test process/strategies will also help to determine a good mix of various tests that result in good coverage and minimize overlapping coverage between strategies as well. No single test strategy can detect all the defects. It is a combination of complementary test strategies that provide good overall coverage, and it's possible to obtain good resulting coverage, even if the access is poor.
By evaluating the maximization of test access in terms of coverage, it can be determined if the actual coverage result is worthwhile. By doing so, the manufacturing test process will be kept lean, and the costs minimized, with cheaper ICT fixtures and reduced cycle time for FPT – which leads to better productivity from the test machines available on the manufacturing test floor.

Design for Test, Test Coverage analysis, DPMO, Escape rate

INTRODUCTION
Traditionally ICT and Flying Probe engineers have looked to increasing accessibility to achieve good test coverage results on a PCB's. Many times, in discussions with test groups, the conversation has turned to getting the most access out of a PCBA; reducing probe size and target size to accommodate ever shrinking designs and higher densities. In many cases DFT is driven entirely by the strive for higher net accessibility. There is of course some validity to this desire – higher test access will generally mean higher ICT & FPT coverage, and the engineer can feel vindicated about these efforts. However, what if the additional access doesn't really result in a higher test coverage, or the increased cost of the access doesn't justify the additional coverage that results. By going to smaller targets and reducing the test probe pitch, cost increases will be seen, as well as potential reliability issues on the fixtures. These will lead to false failures and reduced yield. If the additional costs incurred offer very little, or no benefit, then these costs increases are not money spent efficiently, and with the increasing board densities that are now being seen, evaluating the test access is not sufficient to judge the quality of the test. We need to perform coverage estimation analysis, to understand the resulting test coverage produced by the access and determine the ROI of adding the additional small pitch probes and to determine if the increased coverage is worth the costs.

COST CONSIDERATIONS
By focusing on achieving greater accessibility, ICT, and FPT engineers somewhat overlook the reliability and cost implications of the fixture and test. This is because historically, engineers have been used to reporting the quality of the test as a function of the accessibility, and in fact many customers ask only for a test access report, and feel that by understanding the access, they know what the actual coverage of the board will be, and the quality of the test. By performing a coverage analysis with industry wide metrics, a determination can be made about the resulting test coverage – a much more accurate and meaningful measure of the ability to capture defects, than looking to the usual accessibility.

We must consider metrics that can be used to calculate the test coverage. For an example of this point, let us consider a simple PCBA, comprised of 4 components: 3 resistors and 1 BGA. The three resistors are measured with a very high accuracy by our test, but there is no test on the BGA at all. Can we say that the coverage score is ¾ components for 75%? What if we have access to some of the pins of the BGA, but not all – how much of the BGA is actually tested? We need a test coverage method to weight the coverage and consider what the access that we have, can do for testing of the BGA. We need to consider all of the manufacturing defects within the defect universe including missing components, wrong value, misaligned, incorrect polarity, damaged components, open circuits, insufficient solder, excess solder etc. We must have test strategies that are in place that are capable of catching all of these defects. The ability to detect defects, can be expressed by a coverage level, so that each defect category is aligned with appropriate coverage metrics.

MPSF	PPVSF	PCOLA/SOQ /FAM
Material	Value	Correct
		Live
Placement	Presence	Presence
		Alignment
	Polarity	Orientation
Solder	Solder	Short
		Open
		Quality
Function	Function	Feature
		At-Speed
		Measure

Figure 1. Test Coverage Metrics

The table details industry standard metrics that have been defined by Philips Research (MPS); ASTER Technologies (PPVSF); Keysight (PCOLA/SOQ) and iNEMI PCOLA/SOQ/FAM. These metrics allow the estimation of the theoretical coverage, or measurement of the real coverage, for each unique test strategy, or combination of test strategies.

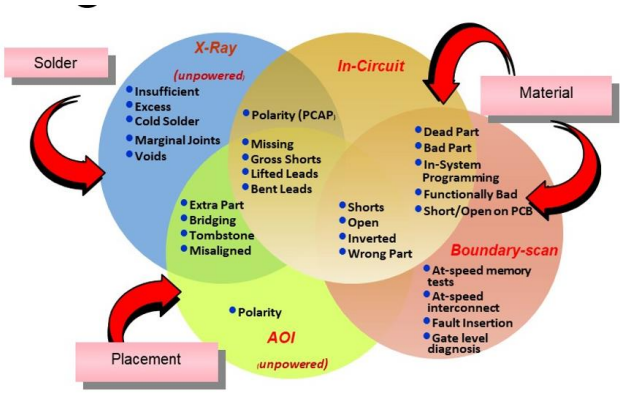

Figure 2: Test Coverage Metrics

ACCESS VS. COVERAGE

From the Schematic capture stage, we can analyze the design and select the required test access points to guarantee good fault coverage. We can analyze for various test strategies and look for optimization to reduce test points, such as using boundary scan to reduce actual physical access that is needed at ICT/FPT. We must simulate the test strategies including any combination of test and inspection machines, which will deliver the highest test coverage possible. This unique combination provides electrical rules analysis, test point analysis, test strategy optimization and test cost modeling, based purely on schematic information. This, in turn, provides valuable layout guidelines that can be used to optimize the Printed Circuit Board layout.

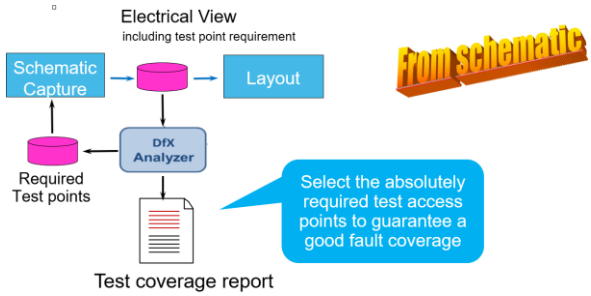

Figure 3 DFT from Schematic

When the board layout becomes available, we can then analyze the physical layout to check fault coverage according to the real physical access that is available on the design. We must confirm with a mechanical DFT analysis that nets that require test access are not compromised by solder mask, component outlines, adjacent probe constraints etc.

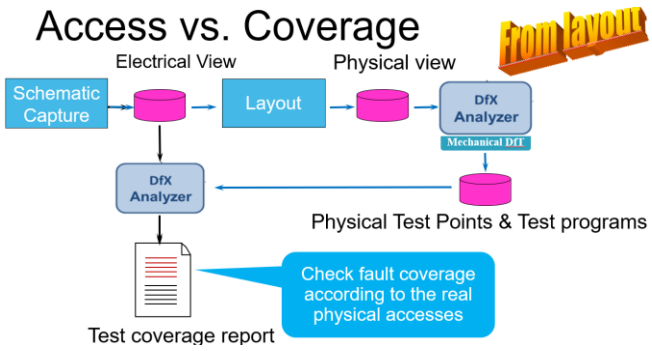

Figure 4: DFT From Layout Stage

CASE STUDY: ADDING TEST ACCESS WHERE IT ISN'T NEEDED

While analyzing a customer board, a difference in accessibility results were noted over what the customer had obtained from traditional access reviews. In investigating the rules that were used for determining the available test access locations, it was discovered that the customer was looking to add access with 50 mil and 39 mil spaced probes on the top side of the board for their ICT testing. So, while this did indeed produce some higher accessibility numbers, the increased coverage turned out to be very minimal. In the table below you can see the additional "small" probes make the access numbers look better.

Table 1. Probe Size vs. Accessibility

DFT analysis	
Probe size	**Net Accessibility**
100 mil	85%
75mil	93%
50mil	97%
39mil	99%

We need to check the test coverage however and see if the resulting 99% access provides better coverage results than the 93% access that could be had by only using 100 and 75 mil probes. After performing the software coverage analysis, with ICT estimation models, it was determined that the additional coverage from the 50 mil and 39 mil probes was not that significant and was already being addressed by another test strategy. While there are times when particular access can be of significant benefit, this particular case was a good example where the additional access accomplished very little. Yet without coverage analysis of the resulting access, a blind decision could have resulted using a fixture and test with these small probes resulting in a costlier process and one that is more difficult to maintain over time.

Table 2. Probe Size Vs. Coverage

DFT analysis		
Probe size	**Net Accessibility**	**ICT Coverage**
100 mil	85%	60%
75mil	95%	71%
50mil	97%	74%
39mil	99%	75%

In the case of this board, there was a diminishing increase in overall coverage when adding the 50 mil and 39 mil access probes. When the test coverage results and reports were illustrated to the customer, it was clear that the added access would not buy them any real benefit, and yet the fixture cost would have increased considerably with the 50 mil and 39 mil pitch probes on the top side of the board. The customer clearly saw the benefit of understanding the test coverage, in order to determine the ROI of the small pitch probes, and to shift their thinking away from traditional test accessibility, as the only way to measure the success of the test.

DPMO

Both DPM (Defect Per Million) and DPMO (Defect Per Million Opportunities) are used for determining the overall quality of the UUT (Unit Under Test), produced from the sample quantity inspected. DPM is a measure of manufacturing throughput: how many bad parts slip through the manufacturing process. DPMO is a measure of performance: how many times a manufacturing defect class occurs. DPMO is also an indicator of which manufacturing process is in need of improvement.

Test strategy and defect occurrences should be linked together so that improved test coverage can be targeted towards defects that occur frequently. A lack of coverage on defects that never occur has no real bearing on the final product quality. It is necessary to go beyond solving surface issues and qualify the product test strategies against the real DPMO that is being observed on the production floor. In this way a true understanding is gained that the test coverage is being employed to find the defects that will be observed on the production floor.

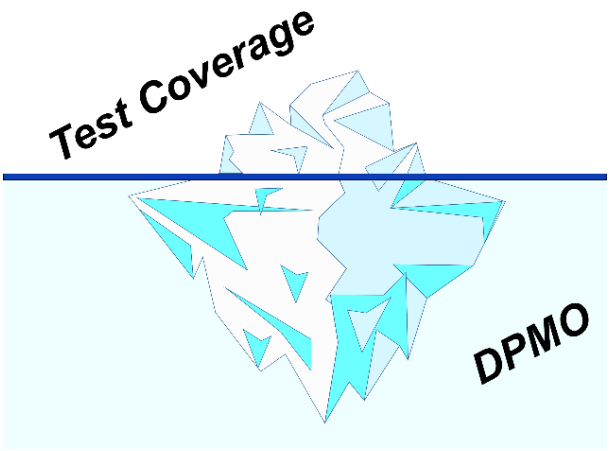

Figure 5: DPMO below the surface

PRODUCTION MODEL AND ESCAPE RATE

Based on our production yield and test coverage computation, it is then possible to calculate important parameters that can be used to evaluate the quality of our test strategy as well as understand the performance of our test at capturing the defects.

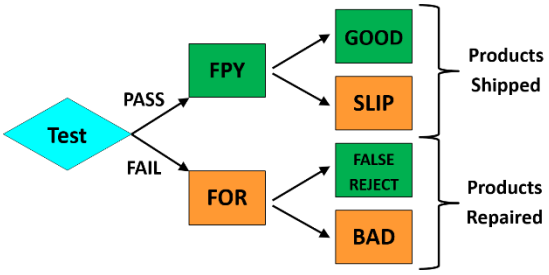

Figure 6: Production Model

"Test" - the test coverage is the percentage of defects that can be captured by a combination of inspection and test machines.

"FPY" - First Pass Yield is the percentage of boards that pass the test.
It can no longer be considered a good measure of the production quality. This is easily demonstrated by a test coverage of 0% which will result in a First Pass Yield of 100%!
"FOR" - Fall of Rate is the number of boards which fail the test. This leads to a though provoking question: I**s a board good because it passes the test?** From practical experience, the following question arises: "Are all failing products really faulty?" And for the same reason we may ask: "Are all products that are shipped, good products?" The answer is clear for both questions: "NO!". "Slip", or the Escape rate, is a key metric and represents the faulty products that will be shipped to the end customer. Ultimately, the "Slip" is how the end-users will measure the final quality. If a PCBA is failing at system test it is because it fell into the escape rate (or slip). If this slip rate is much higher than expected, then there are two possible reasons why this situation occurs:

- The DPMO figures are higher than expected.
- The combined coverage is lower than optimal.

Incorrect DPMO figures are probably due to limited defect traceability, or incorrect root cause analysis.

COMBINED TEST COVERAGE
While alluded to above, and in the case study, we need to take advantage of the combination of test strategies to achieve our desired levels of test coverage. No single test strategy is capable of detecting all of the defects that occur in the defect universe. We need to look to each strategy and understand what its capable of detecting. We can then combine these test strategies and look at the union or sum of the test coverage coming from each strategy. By selecting a combination of test strategies, we can then achieve our desired total test coverage which is capturing the majority of the defects that we expect to see.

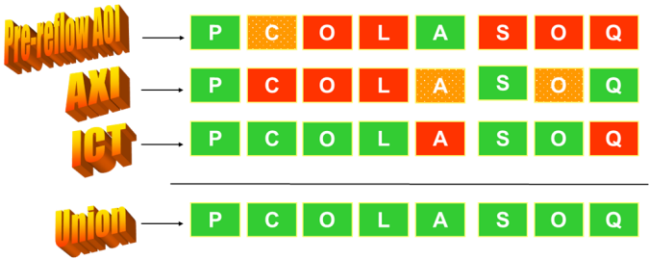

Figure 7: Combining Test Strategies

IMPROVING ACCESS WHERE IT WILL BE THE MOST BENEFICIAL

One question which has long been asked of test engineers and DFT engineers when a test accessibility review is provided back to the layout/design group, is the following: If some additional access could be added to the design – which nets without existing access would provide the greatest benefit to the test coverage? Usually this means manually providing a criticality listing of the nets with missing access, so that the layout engineer can try to add access to the most critical nets. How is the criticality determined? One method is to examine the potential uncovered defects. Using software tools, we can understand the devices with the highest possible escape rate, uncovered DPMO if you will, to add access where it will be the most beneficial for improving overall ICT/FPT coverage, and reducing the slip rate. Using this automated process, a list of access which will be the most beneficial can be generated for the layout engineer to try and address, herby addressing this longstanding question. In some cases, access can even be removed where it is not providing coverage enhancement, and the access re-assigned to more critical nets which will result in higher coverage, yet with the same probe count in the fixture. Now the coverage has been maximized without increasing the costs of the test/fixture or causing reliability implications. Software tools allow all of these scenarios to happen on the virtual test line or Digital Twin of the test line, so that the engineer can decide on the best allocation of test access before the test development and fixture build occurs. This provides much greater visibility to the outcome and overall quality of the test (greater yields and reduced slip rate, or bad boards passing the test and making it to the customer).

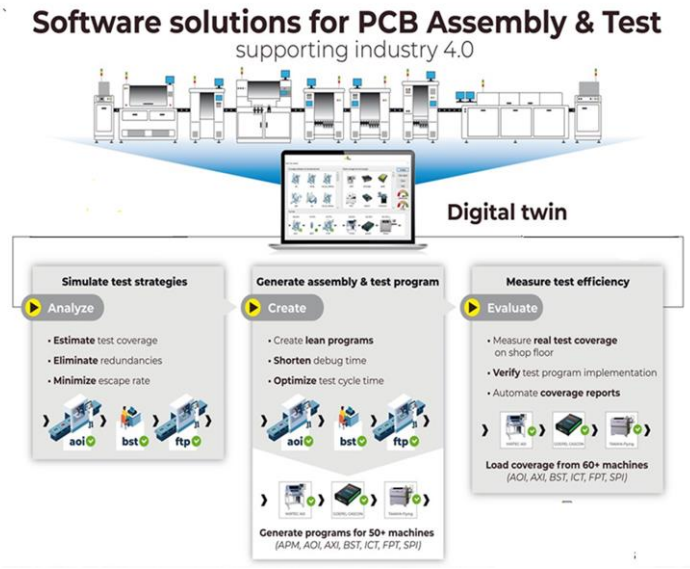

Figure 8: Digital Twin of the Manufacturing Test Line – Create a virtual Copy for Decisions to be made

CONCLUSION
As circuit board layout continues to move to higher densities, traditional ICT/FPT accessibility becomes more difficult to obtain and comes at a higher price for test development and maintenance over the lifetime of the product. Software tools should be used to evaluate the overall test coverage of the board, from all test strategies

being employed, and understand if driving towards more accessibility is actually necessary. Accessibility alone for ICT or flying probe tests shouldn't be the only consideration for how well the board is tested. Employing an industry wide metric with software tools to determine the overall test coverage of a PCBA is the way to guarantee a quality product while minimizing test costs. As companies have a capital investment with their ICT and FPT machines, determining the best test access that is required to achieve optimal test coverage results, is the way of getting some ROI on the capital investment that has already been made. Qualifying this coverage against the true defect opportunities (DPMO) that are on the production floor will result in coverage that meets expectations and reduces the bad product that is leaving the shop floor. This will ensure that there is no significant cost of poor quality effecting the bottom line by the shipment of bad product.

Understanding potential uncovered defects or slip rate and the parts that are included in that is the key to driving for higher test coverage where it will have the most benefit. In some cases, its possible to re-allocate access in a more beneficial way and maintain the same number of ICT/FPT access points but using them in a better way to increase test coverage. All these ideas can be explored using software tools and creating a virtual copy of test line to fully gain an understanding of what each test strategy is able to do and what defects you will be detecting. Clearly, driving for simply the highest test accessibility is no longer the way to achieve good test results or the most efficient use of the test equipment that is available.