Calculation of Board Test Coverage

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In the past

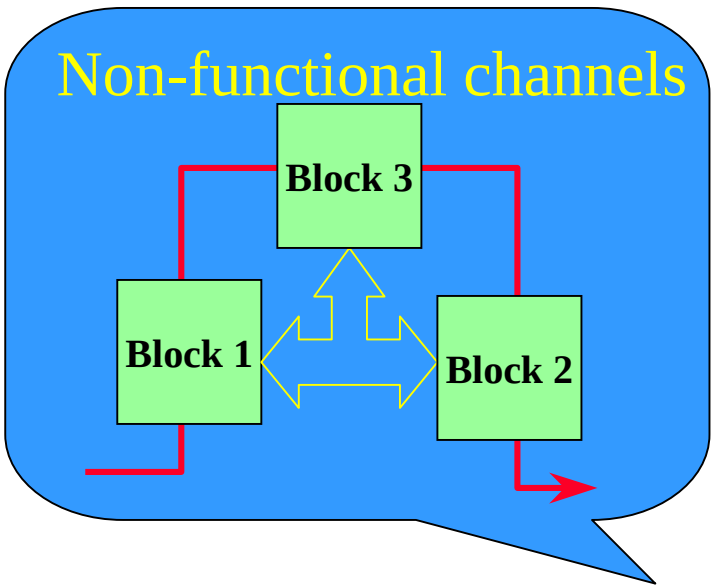
- In-Circuit Test was available for testing board with full nodal access.
- The Test Strategy was build around a single test step.
- Test Coverage was a percentage of what is tested:

$$\text{Test coverage} = \frac{\text{Number of devices with test}}{\text{Total number of devices}}$$

- 2-Pins Resistor has the same importance as an IC!

The world changes

- **Electronic design and production changes:**
  - Functional complexity of the electronic boards.
  - Staggering board density.
  - Outsourcing of board production.

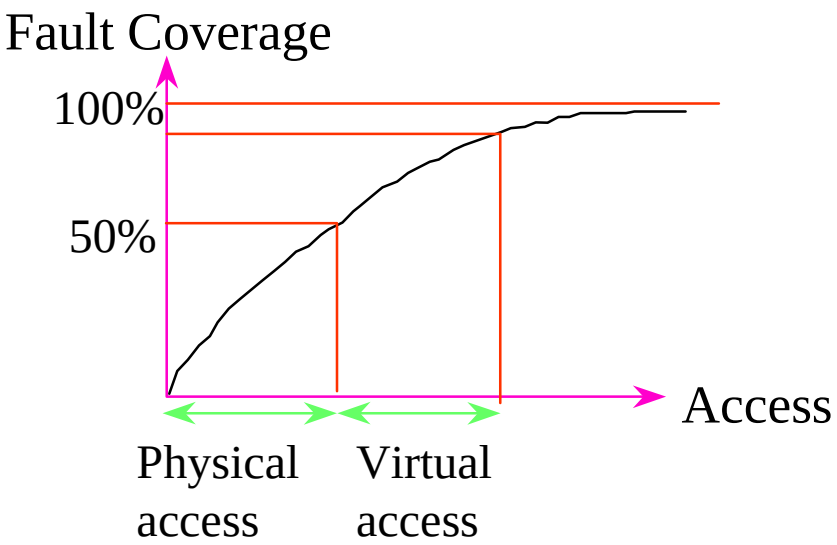


SMD, fine pitch,
BGA, buried via

We buy good boards

Physical accessibility

- **Loss of physical accessibility promotes test techniques.**
  - Automated Optical Inspection (AOI)
  - Automated X-ray Inspection (AXI)
  - Flying Probe Test (FPT)
  - Boundary-Scan Test (BST)
  - Functional Test (FT)



We buy good boards

- Is a board good because it passes the test?
- What is the acceptable percentage of faulty boards that could be delivered with the “good boards” label?
- What is the quality level of a complete system if the quality of each individual board is not under control?

Require formalization of production defects and test coverage.

Today

- The Test Strategy involves several test steps distributed in the production line.

- Consider a production line including an AOI, BST and ICT, when a serial resistor is located between two Boundary-scan devices:
  - AOI - Camera checks presence.
  - BST - An electrical signal is propagated through the resistor.
  - ICT - Measurement of the resistor value.

Chinese watch syndrome

A man with one watch knows what time it is.

A man with two watches is never sure.

- Several different metrics make the comparison and combination impossible.
- Coverage must be readable from design to production.

Defects

- **Typical defects**

Missing components **Wrong value**

Misalignment

Polarity **Tombstone**

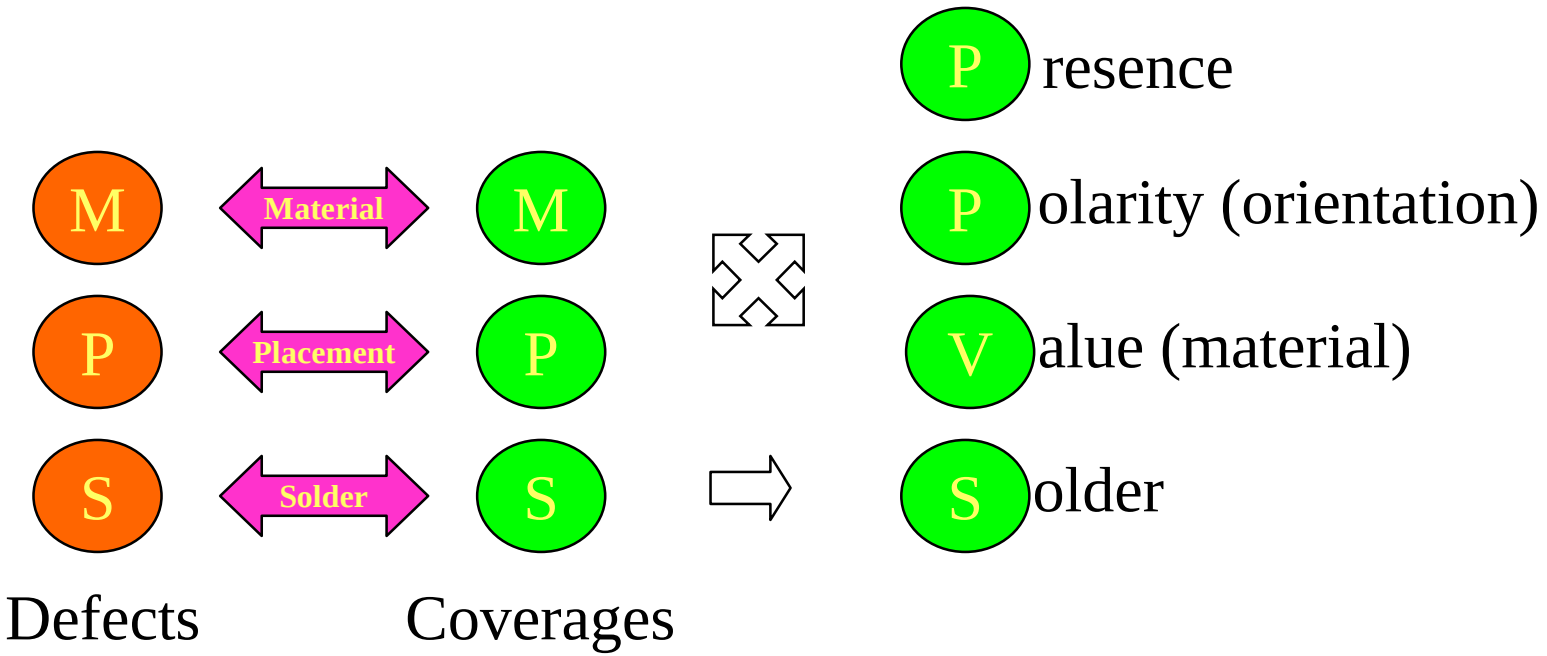
Opens **Broken leads**

Insufficient solder **Shorts**

- **Manufacturing flow**

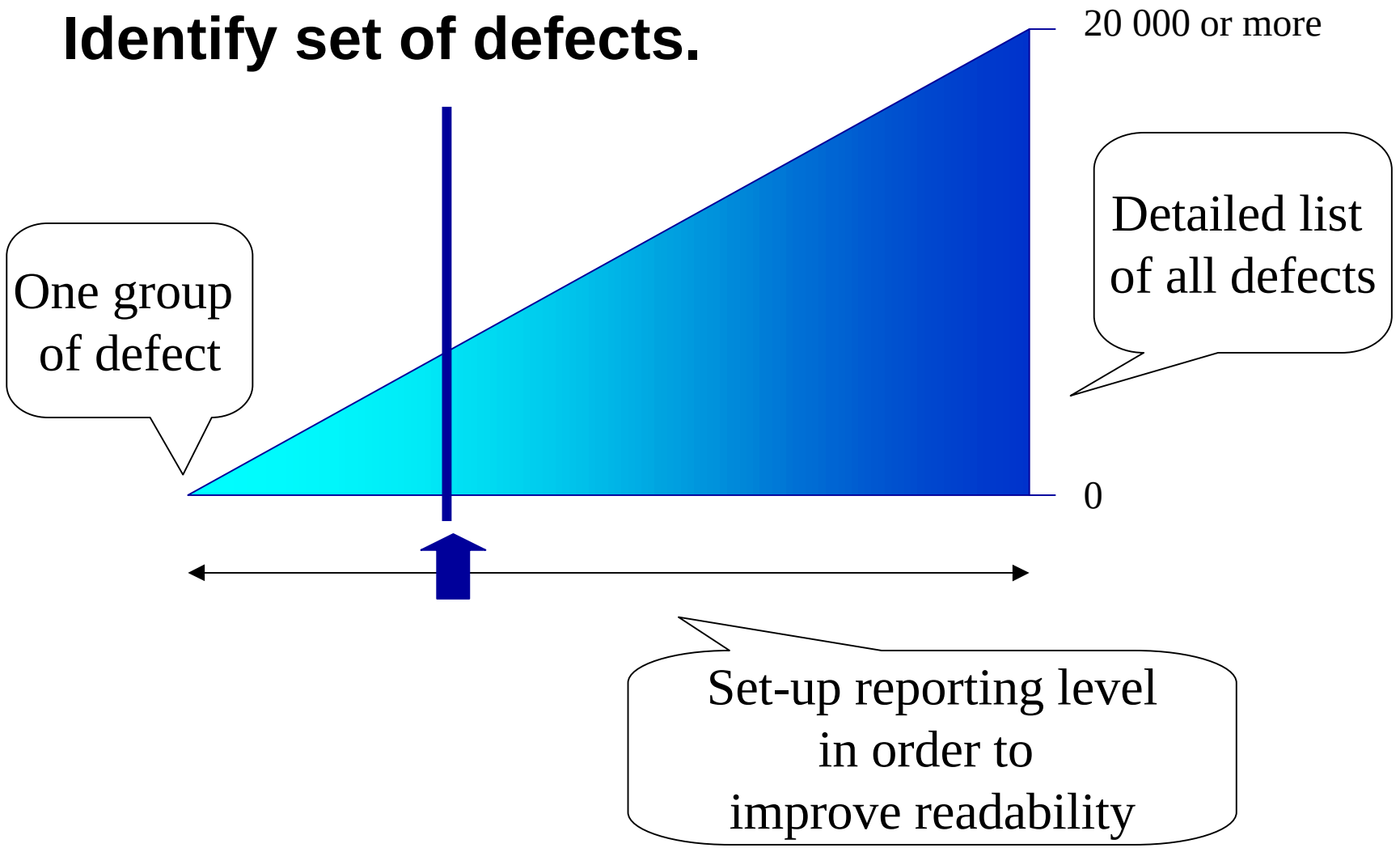
Defects | Coverages

- The ability to detect defects can be expressed with a number: coverage.
- Each defect category fits with its test coverage:



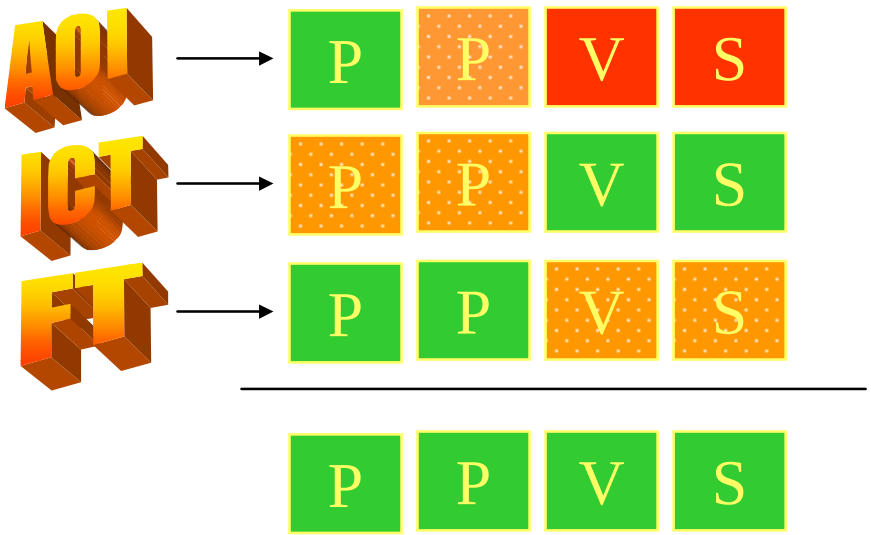
Defects | Coverages

- **Manage each defect as a key.**
- **Identify set of defects.**



Combination of the facets

- Each test technique brings a certain ability to detect the defects.



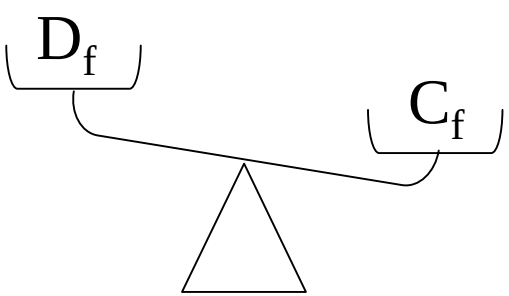
- Good coverage = combination of tests

Weighted coverage

- For each category (MPS) of defects (D), we associate the corresponding coverage (C).

$$\text{Effectiveness} = \frac{\Sigma D_M \times C_M + \Sigma D_P \times C_P + \Sigma D_S \times C_S}{\Sigma D_M + \Sigma D_P + \Sigma D_S}$$

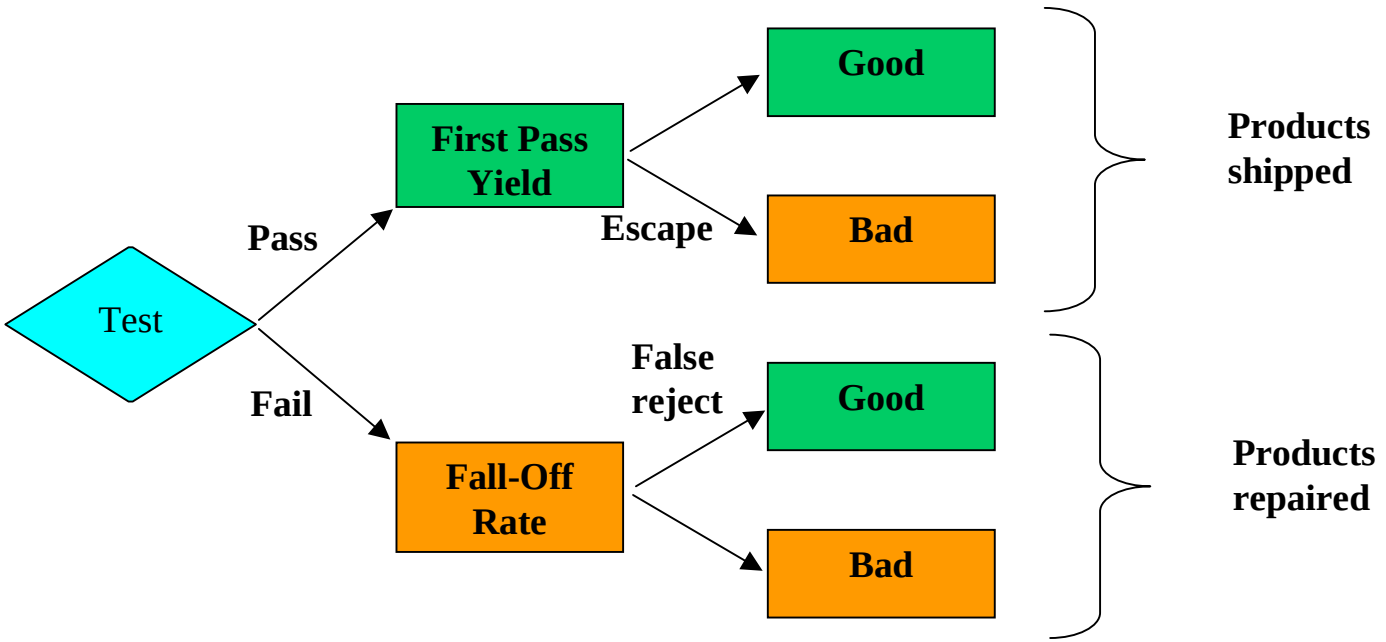
- The PPVS model is based on a coverage balanced by the defects opportunities.



We need a better coverage where there are more defect opportunities!

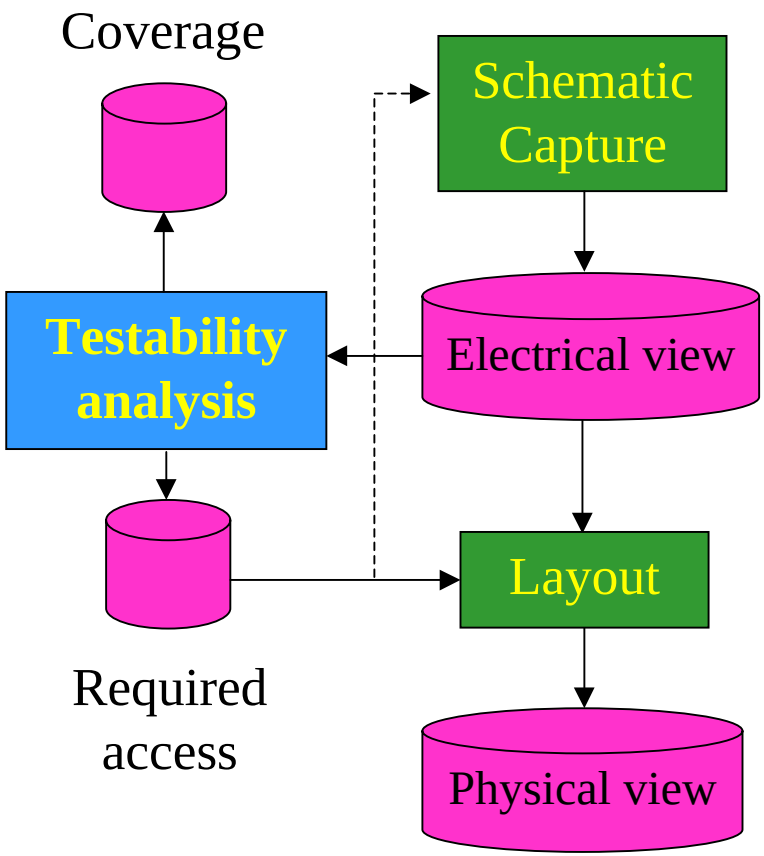
Production model

- Summarize the facets in a limited set of numbers that will guide the test strategy choice.



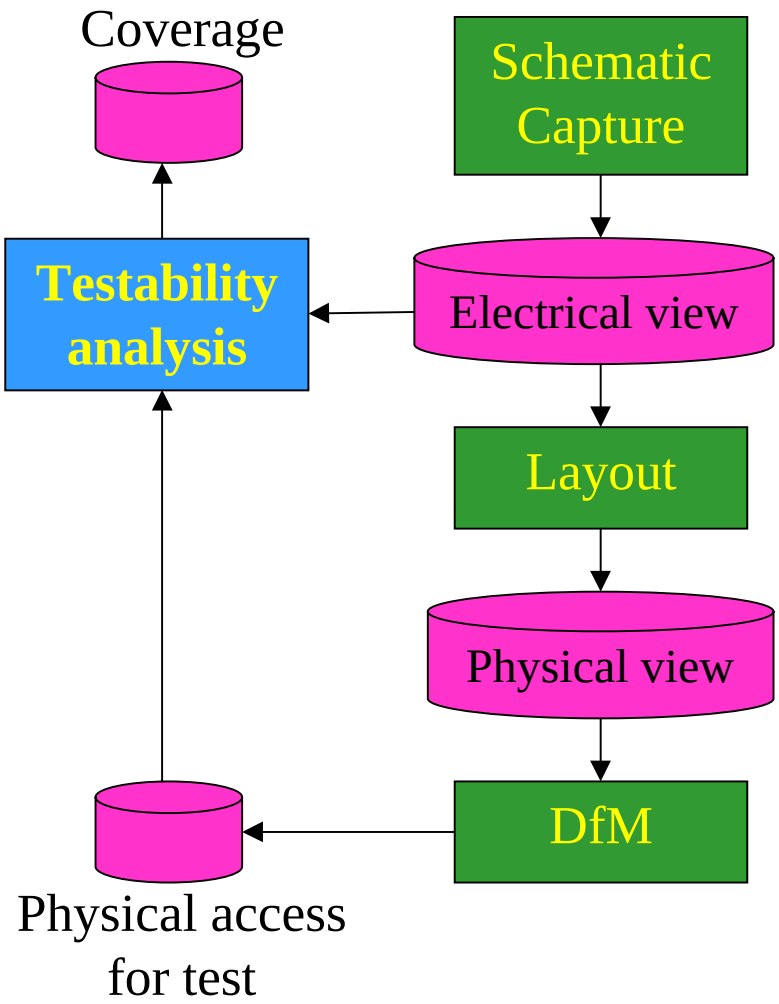
- The “Escape” is an effective way to measure the manufacturing quality.

From schematic capture

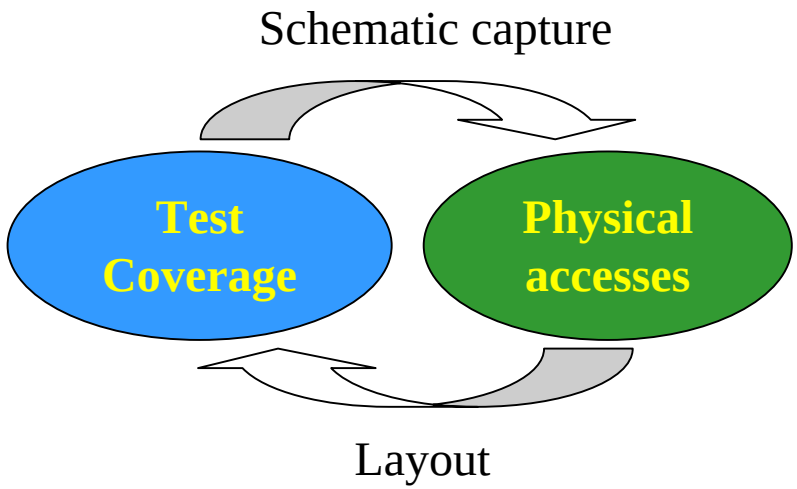


- Testability rules violations limit the test coverage.
- Accessibility requirements are back annotated prior to layout, ensuring that the required physical accesses will be available where they are mandatory.

From layout



- The copper area having the required properties will be used as access points for In-Circuit Test or the Flying Probe Test.



From a test program

- Analysis of a test program allows, in many cases, determination of the real coverage.
  - The “step-by-step” analysis of the test program determines the measurement type and consequently the defects that can be detected.
  - The test coverage report - human-readable.
  - The test & coverage report - machine-readable.

Addition of a new class of defects,
update of the calculation method
of the test coverage
are clearly simplified.

From a test program

- Are all types of tester able to report board coverage?

- A tester should report only:
  - List of measurements: a measurement doesn't always produce coverage due to the electrical environment (passive components in parallel, diode on digital inputs…)
  - List of simulated faults and detection: named fault inject on In-Circuit Tester.

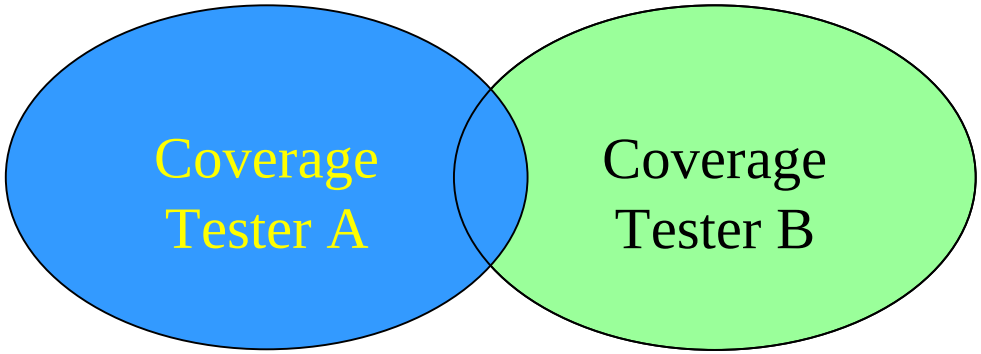
- What about fault grading an AOI or an AXI?

Using coverage

- Predictive estimation
  - From a part list, a net list and a tester model, the predictive estimation determines testable configurations and calculates test coverage.
- Declarative estimation
  - People working on test program specification or development declare the elements that are tested during each test stage.
- Validated estimation
  - The framework of test program development simulates defects on the physical board or a data-processing model and determines detected defects.

Union

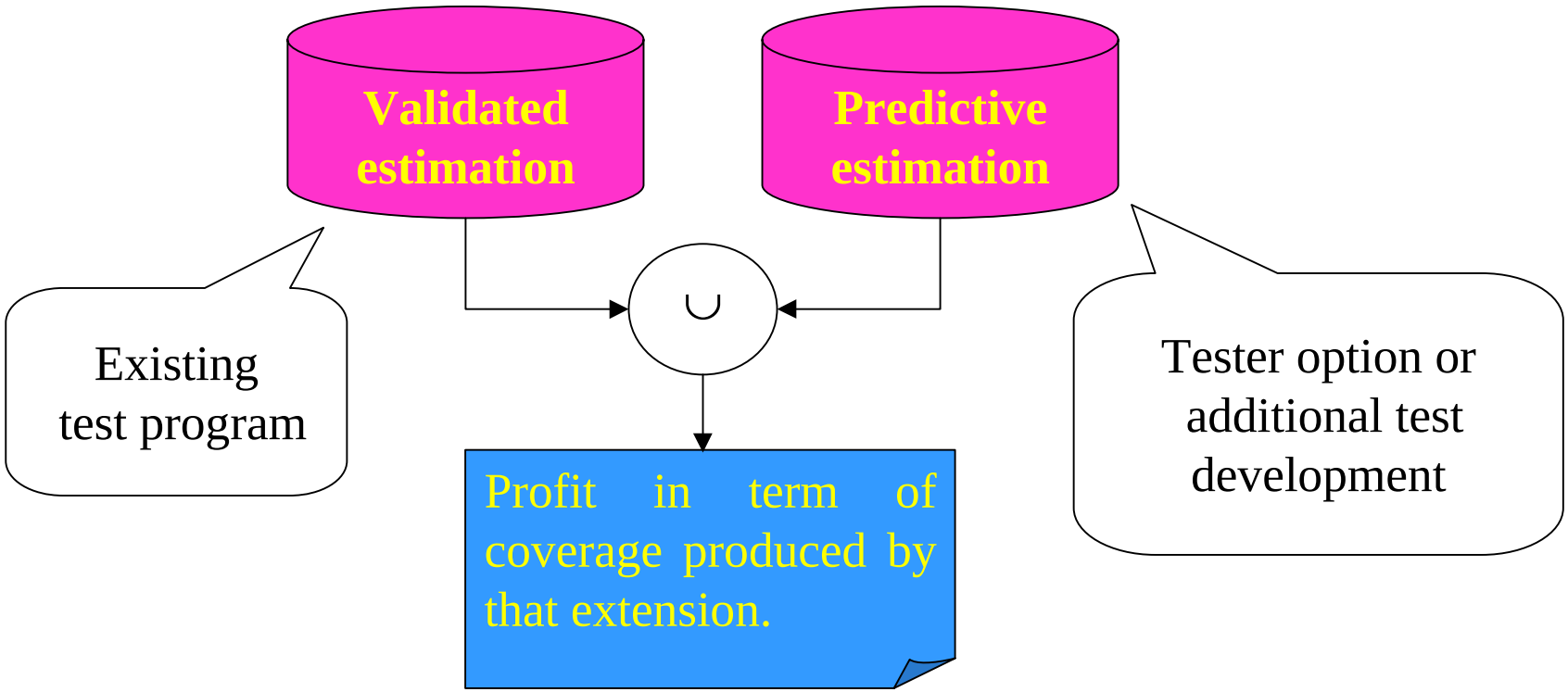
- The facets follow group theory in mathematics.



- Union
  - Increase in total coverage: $C_{total} = C_{TesterA} \cup C_{TesterB}$.
  - Some defects remain undetected.
  - Any overlapping of the test techniques produces redundancies: Redundancy = $C_{TesterA} \cap C_{TesterB}$

Other application of Union

- Simulate the improvement of an existing program by hardware or software extension.

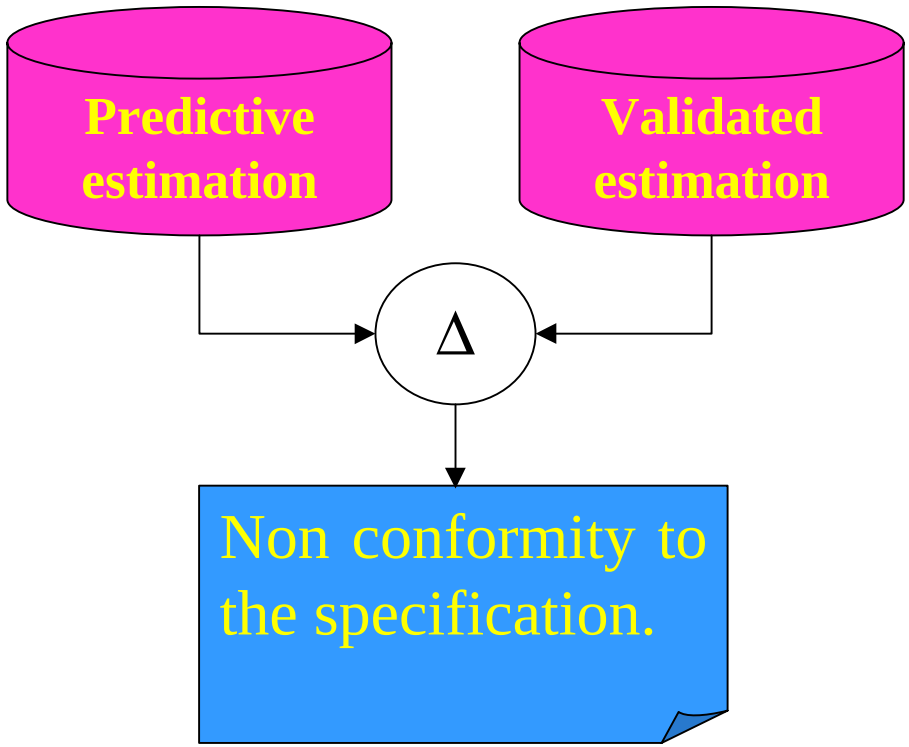


Comparison

- The comparison places in parallel two test strategies which produce different test coverages. Choosing one or the other is based on various criteria:
  - The “Escape Rate” that constitutes the effective measure of the test coverage.
  - The level of redundancy that has to be maintained between the various test stages in order to ensure a good level of diagnosis. The test coverage represents only the ability to detect the defect, not the ability to diagnose it.

Difference

- The predictive estimation is used as specification for the development. Once the test program is developed, the validated estimation is available.



Conclusion

- From design, during production and in a more general way, through the whole life cycle, coverage estimation permits the test process to be optimized.
- By deploying various testers in the best order, at the best time, with controlled levels of redundancies, costs can be reduced and quality levels raised.
- The economic challenges are critical: the tools to meet them are available

TestWay summary

- DfT from Schematic to production.
- Electrical rules checking automation
- Integrated platform for coverage prediction and measurement
- Support mixed-vendor testers in a test line since 1998!
- Test Point Saver and Test program optimization
- Tester interface

End of the presentation