‘Kontron’ reaps the benefits in using TestWay for test coverage analysis and standardizing their DfT methodology

Robert Dubois, DFT Architect at Kontron Canada, wanted to have more visibility of test coverage for providing more accurate information on the coverage achieved each test stage, in order to evaluate more accurately the test cost for each type of unit. After evaluating the ‘TestWay’ electrical DfT and Test Coverage analysis tool from ASTER Technologies, Kontron realized the immediate benefits in standardizing on a methodology for calculating test coverage across multiple test strategies.

In today’s electronic design and manufacturing climate, there is an increasing emphasis to shorten time-to-market, improve product quality and lower cost. The ability to verify that PCB designs have been developed with adequate DfT (design-for-test) in mind and determine the most effective test strategies based on accurate fault coverage predictions, is crucial in improving competitive advantage, lowering cost and determining the quality of a product.

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Test coverage calculations for PCB (printed circuit board) are becoming increasingly important as a key indicator in determining the quality of a product. In the majority of cases PCB structural test strategies that include test and inspection techniques such as in-circuit test (ICT), flying probe test (FPT), automated optical inspection (AOI), automated x-ray inspection (AXI) or boundary-scan test (BST), are perfectly adequate in detecting the majority of manufacturing structural faults.

Increased cost savings and higher production yields can be achieved by improving test effectiveness in terms of fault coverage.

“In my experience telecom customers are usually very demanding about test coverage and in understanding the coverage calculation used. Subsequently, it is very important to present a standardized approach in providing detailed coverage information, for each stage in the manufacturing process that meets the customers expectations.” says Dubois.

TestWay’s electrical DfT checker enables designers to validate designs at the schematic capture stage, to ensure that adequate measures have been included to comply with the manufacturers test requirements. This is particularly important when adopting strategies such as boundary-scan, where adequate DfT must be correctly implemented at the design stage. Similarly, test engineers can utilize TestWay’s test coverage analyzer to predict fault coverage aligned to various test strategies, and identify where fault coverage and testability improvements can be made.

“When you work for a multinational company, a key issue is to standardize the DfT methodology across all sites, even inside your own test engineering department. Simply because, each person may have a personal approach for implementing DfT and in evaluating test coverage. By using a defined methodology for DfT checking and test coverage analysis you can guarantee more standardized information,” says Dubois.

“It is absolutely imperative that we ensure our designs have adequate testability, because it is often impossible to respin a design due to the engineering cost and availability of design resources. TestWay will definitely help us to save time and money in providing comprehensive testability reviews and ensuring that we do not overpay for certain types of test, and help quantify the ‘test overlap versus the price’. More importantly, it allows us to evaluate the quality of test programs, either developed in-house or by our subcontractors. Providing complete visibility of the test process in order to provide us with the knowledge that our products are adequately tested.”

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