BOARD TEST - COVERAGE ANALYSIS
Is a board "good" because the test passes?

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ABSTRACT

Test coverage is a key qualification tool for driving schematic design, board layout and test program development for enabling the best production yield.
The various test coverage methodologies used within the industry are based on the MPS model; however two other representations, PCOLA/SOQ and PPVS have been developed in defining how the coverage metric is calculated using complementary fault models. These test coverage models have been invariably used to determine the level of test coverage using structural test strategies, such as AOI, AXI, FPT, ICT, and Boundary-Scan.
This paper also presents a further development that takes into account functional test coverage by expanding the MPS model to include design and function (DMPSF). Whereby a functional board test (FT) can be used to validate the design and complement the structural coverage.

KEYWORDS: Design-for-Test (DfT), Design-for-Manufacture (DfM), test coverage, coverage metrics, PCOLA/SOQ, PPVS, structural test, printed circuit board (PCB), functional test (FT), board defects, structural defects, boundary-scan test (BST), automated optical inspection (AOI), automated x-ray inspection (AXI), in-circuit test (ICT), flying-probe test (FPT), surface mount devices (SMD), chip scale packaging (CSP), direct chip attach (DCA), parts per million (PPM) and no fault found (NFF).

INTRODUCTION

The electronics industry is characterized by a continuous design evolution. During the last fifteen years, three main factors have resulted in the questioning of Design for Test and Design for Manufacture methodologies.

- Functional complexity of electronic boards.
- Staggering increases in board density (SMD, fine pitch, BGA, CSP, DCA, buried via) etc.
- Outsourcing of board manufacture.

FUNCTIONAL COMPLEXITY

Component complexity largely contributes to electronic board complexity i.e. the numbers of sheets that make up the schematic diagram and the number of interconnections continually grow, which questions the traditional analysis methods and the tools.

Testability must be accounted for during the preliminary architecture definition, in order to ensure that adequate test coverage is provided at each stage during manufacture and in the repair cycle. As a result, test coverage calculations for printed circuit boards (PCB) are becoming increasingly important as a key indicator in determining the quality of a product.

BOARD DENSITY

The evolution of component packaging technologies has resulted in an increase in device IO and a staggering increase in board density due to smaller components that has lead to a growth in the number of device interconnects. Subsequently, this has resulted in a loss of physical access that is necessary for traditional structural test strategies such as In-Circuit test.

However, in the majority of cases PCB structural test strategies that include test and inspection techniques such as automated optical inspection (AOI), automated X-ray inspection (AXI), in-circuit test (ICT), flying probe test (FPT), and boundary-scan test (BST) are perfectly adequate in detecting the majority of manufacturing structural faults.

There are however, situations where the optimum test coverage is not achievable through structural testing alone, or it may be that the current test strategy provides inadequate structural test coverage due to limited access.

Under these circumstances, it may be beneficial to predict the test coverage contribution provided by functional board test (FT) to detect structural defects, not only during production but also during the product maintenance phase.

OUTSOURCING PRODUCTION

The electronics industry provides its subcontract manufacturers with a simple message: "We want to buy good boards".

This approach however, prompts some questions:

- Is a board good because it passes the test?
- What is the acceptable percentage of faulty boards that could be delivered with the "good boards" label?
- What is the quality of a complete system if the quality of each individual board is unknown and not under control?

MANUFACTURING FAULTS

The manufacturing process is not free from introducing faults, due to the capabilities of the equipment and the process used.

Typically, the defect universe comprises of the following defect categories:

- Missing devices
- Wrong value, 10K instead of 100K
- A dead device e.g. ESD damaged or cracked device
- Incorrect polarity, rotated 180 degrees
- Device misalignment
- Tombstone effect
- Broken lead
- Short between adjacent pins caused by solder bridge, bent pins, or mis-registration
- Open solder joint
- Poor solder joint, due to excessive, insufficient or malformed solder

Subsequently it is important to categorize these faults in relationship to a group of test coverage facets that provides a logical link with the production process, and allow the model to be clearly understood by designers, project management and production people. These test coverage facets are defined by three accepted de-facto standards for modelling test coverage:

MPS - Philips Research[1]
PPVS - ASTER Technologies[2]
PCOLA/SOQ- Agilent Technologies[3]
The list of faults described within the defect universe can be further sub categorized as:

- **Defects** – that can be detected by a test, or fixed by a repair.
- **Deviations** – that can be located by inspection and are fixed by process tuning.

For example the [A] Alignment and [Q] Quality facets described in the PCOLA/SOQ model are deviations in the production process that can be resolved by fine tuning the process.
However, if the deviation becomes problematic enough, it becomes a defect. The problem then becomes, how to determine at what point the deviation becomes important, which is one of the fundamental reasons for the false reject scenario with inspection tools.

DEFECT UNIVERSE
It is important to understand how the defects defined in the 'defect universe', correlate to the individual facets within each of the test coverage models. This will help to understand the reasoning in predicting the test coverage for a functional board test strategy.

This list of defects must comprise of manufacturing faults that are recognized consistently throughout the electronics industry and accepted as 'the defect universe' for providing a framework for test coverage metrics. Studies have been made and published in technical papers[123] that identify a number of ways to represent test coverage based on the concept of multiple facets.
In trying to rationalize the various test coverage models, Lotz[2] identified two major problems that needed resolving:

1. How many facets are necessary to represent the most complete test coverage?
2. Consolidation of the facets into a single value.

The model we will use for computing test coverage has to be consistent with the manufacturing process. It is important that the model is easy to understand for design and manufacturing engineers.
The manufacturing flow comprises of three stages that determine; the supply of correct materials, the correct placement of components and the soldering of components to the PCB.
The correlation between the 'defect universe' defined by the various models and the different test coverage facets are shown below.

Figure 1: Manufacturing flow

This high level (MPS) representation of the manufacturing process can be further broken down within a hierarchical tree flow to obtain lower level detail like PPVS or PCOLA/SOQ or even expanded to show additional sub-criteria:

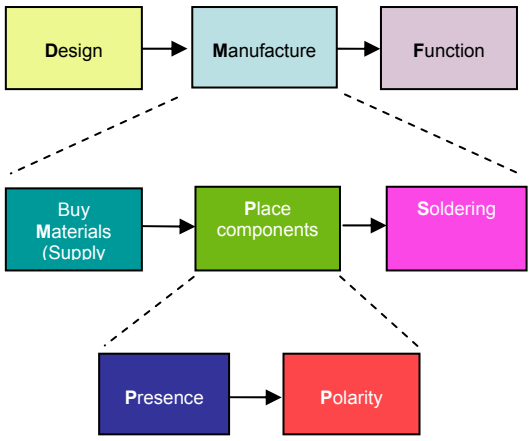
- Absence (not fitted DNP components),
- Downloaded (Flash, FPGA, µC),
- Component revision labeling,
- Solder shape,
- Solder density (voiding in lead-free soldering).

MPS [1]	PPVS [2]	PCOLA/SOQ [3]
Material	Value	Correct Live
Placement	Presence	Presence Alignment
	Polarity	Orientation
Solder	Solder	Short Open Quality

When functional test is considered not only as a test strategy for detecting structural defects, but also as a validation of the design function to determine that the board-under-test (BUT) is fit-for-purpose; we need 3 main defect classes:

1. **Design defects** – that have to be detected by a design rules checker (DRC), or by electrical DfT or DfM.
2. **Production defects** – MPS or PPVS model.
3. **Functional defects** – these defects are not specifically attached to a single component, but to a block of components

Figure 2: DMPSF Flow



If we now take these additional defect classes into account, the test coverage model now becomes **DMPSF**: **D**esign, **M**aterial, **P**lacement, **S**older and **F**unction.

CONCEPT OF COVERAGE

All the methodologies that have been discussed (MPS, PPVS, PCOLA/SOQ) provide an equivalent framework for determining test coverage metrics, but identify extra sub-categories to provide additional coverage information.

In order to define what is meant by the concept of coverage, we can use the example of a serial resistor that is located between two Boundary-Scan components; several methods can be considered to test this component:

- *Simple AOI* – the camera checks the component presence on the board; no physical access is required, there is no value measurement and no solder checks.

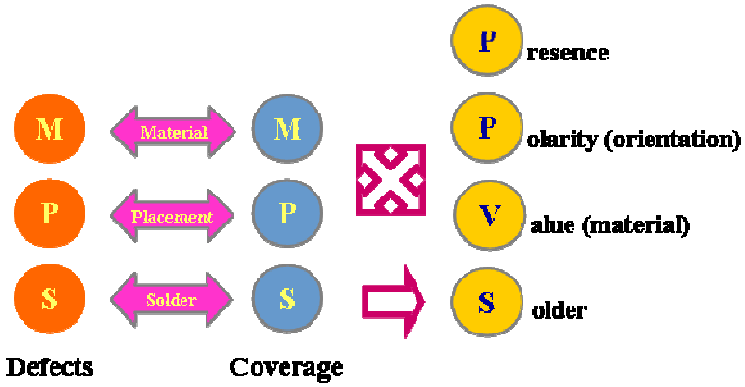
- *BST* – an electrical signal, propagated through the resistor checks for component presence and its solder; no physical access is required and no value is measured.
- *FPT or ICT* – measurement of the resistor value checks the component presence, plus the solder and component value, but physical access is required.

This example highlights two key points:

- The concept of "tested is different from one tester to another. It is mandatory to clarify the meaning of "tested".
- Testability is the search for an acceptable compromise between design and test; in the above example, if you want to test the value of resistance, physical access is required.

With each class of defect, it is important to associate a coverage value to indicate if the defect will be detected.

Figure 3: Coverage = Mirror of defect



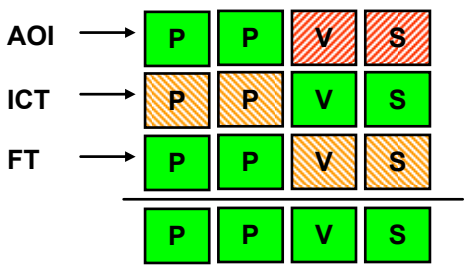
Within certain branches of the industry, additional classes of defects such as: Dynamic, Programming, Jitter, Crosstalk… could be needed.
However, for each new class of defects, it is mandatory to set up the corresponding coverage facet in order to preserve the mirror effect.

COMPLEMENTARY TEST COVERAGE

Each test technique has the ability to detect some of the defects defined within the 'defect universe'; however, no single solution is capable of detecting all the defects. This can only be achieved by a combination of complementary test techniques to provide the optimum test coverage as defined in the PPVS test coverage model.

In figure 4, we show the PPVS coverage for a combination of test techniques that comprise of structural tests; visual inspection; electrical process tests and functional (performance) tests. From this a coverage value can be predicted that represents the ability to capture all the defects.

Figure 4: Complementary test coverage

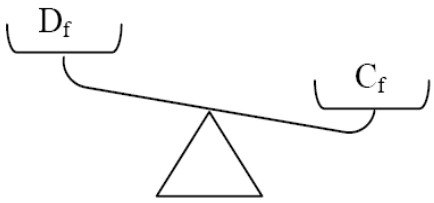


DEFECT OPPORTUNITIES

It is also important to consider in any test coverage predictions, the associated defect rates for the components used within a design. This information can be obtained either from the International Electronics Manufacturing Initiative (iNEMI) http://www.inemi.org, or from the Smart Group PPM (Parts-Per-Million) Monitoring website www.ppm-monitoring.com.

This information is useful in providing defect values based on manufacturing data obtained from industry wide PPM monitoring projects, and is particularly useful when starting the analysis on new designs and processes. Quality management tools, such as QUAD[4] can be used to collect the DPMO (Defects per Million Opportunities) data from local manufacturing facilities, so that yield predictions can be calculated based on real-time process data.

Taking into account DPMO data does not complete the picture, because although test coverage confirms that we can catch defects, we need to balance this with test efficiency (weighted coverage) that informs us whether the test strategy is consistent with the defect universe.
The PPVS model is based on test coverage balanced by the defects opportunities (DPMO).



The weighted coverage can be calculated by:

$$Coverage = \frac{\sum D_M \times C_M + \sum D_P \times C_P + \sum D_S \times C_S}{\sum D_M + \sum D_P + \sum D_S}$$

Where for each category of defects (Df, f ε {M, P, S}), we associate the corresponding coverage (Cf, f ε {M, P, S}).

The previous formula can be further expanded to cover "Maintenance test", where the calculation is made using the Lambda (λ) value linked to 'failure in time', instead of the DPMO value in production.

$$Coverage = \frac{\sum \lambda_F \times C_F + \sum \lambda_B \times C_B}{\sum \lambda_F + \sum \lambda_B}$$

Where for each category of defects (λf, f ε {F, B}), we associate the corresponding coverage (Cf, f ε {F, B}):

- Where *F* means component function:
  Failures relating to the function of the part i.e. value drift; dynamic characteristic drift; dysfunction etc. Some of these defects can be detected by ICT or BST, but functional test is more suitable.
- Where *B* means component border:
  Failures relating to external pins i.e. broken joints; broken bonding; defective input/output buffer etc. These defects are detected by structural tests such as ICT & BST.

A number of assumptions are considered in estimating maintenance test coverage, such as:

- Boards shipped to the customer are considered good, so all devices are present & correct.
- When a board fails in the field it is not due to a missing or mis-orientated part.

COVERAGE FROM A TEST PROGRAM

Analysis of the real test program or test coverage report produced by a test system, allows in many cases, verification of the real coverage.
In the field of test coverage reporting, the following cases are examples of the format in which test coverage is available:

1 **Test program**: for AOI, AXI and FPT testers, the "step-by-step" analysis of the test program determines the type of measurement and consequently the defects that can be detected.
2 **Test coverage report:** it presents the covered elements synthetically in an ASCII format, like XML database or table describing the coverage by pin, component and net.

Test coverage reports based on a formal syntax, transfers pin level information to the testability analysis tool, such as those provided by TERADYNE, AGILENT, AEROFLEX, VISCOM, SIEMENS, ITOCHU and all the leading boundary-scan tools vendors.
It provides an estimation of the total coverage provided by the testers used within the production line, but without any approximation based on the combined test coverage.

FUNCTIONAL TEST (FT) COVERAGE

A functional test solution is developed primarily within the hardware design environment as a test vehicle for verifying that a PCB meets its design criteria.

Once the design validation and prototyping testing phases are complete, the test vehicle is transferred to the Test Engineering department to be used as a functional test platform to verify that manufactured products meet their performance specification and are 'fit for purpose' to be shipped to the customer. The functional test stage is the final PCB quality gate.

However, functional testers are a challenge because:

- It is extremely difficult to predict test coverage provided by a test program unless fault simulation has been undertaken.
- Measurement statements from the test report are difficult to correlate against defects.
- Fault diagnosis is either extremely limited or in some cases non-existent, with the majority of tests simply providing PASS/FAIL status.

The estimation of the defect coverage provided by functional testing often requires far more elaborate calculations. If coverage information is available for each of the defect classes, then it makes sense to reuse this information in the functional test coverage calculations across all designs.

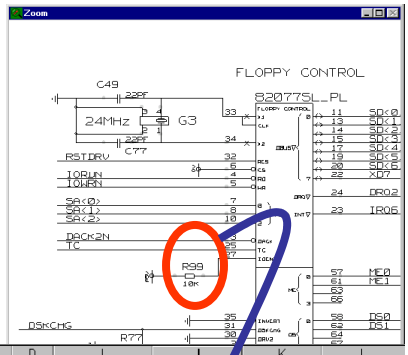
This paper describes two methodologies to create a functional test coverage report.

1. **Declaration** – using schematic and/or layout viewers as the test coverage input device.
2. **Inheritance** – test reuse in a hierarchical design flow where a functional block is associated with test coverage calculations.

These methodologies are also applicable for system test, embedded test or stress test.

DECLARATION METHOD

The **Declaration** method utilizes information supplied by the user relating to test coverage predictions associated with specific functional blocks including the importing of component reference designator and pin number.
Manual importing of this type of data in the form of a MS Excel spreadsheet is prone to human error, which often results in incorrect information being entered.

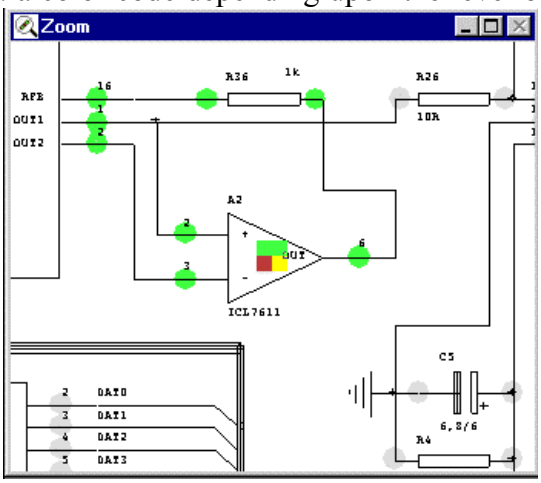


	A	B	C	D	I	J	K	L
1	ref	type	complexity	pin_cnt	coverage_presence	coverage_polarity	coverage_value	coverage_solder
2	R96	680R	RLC	2	100.0	100.0	0.0	100.00
3	R97	680R	RLC	2	100.0	100.0	0.0	100.00
4	R98	1K	RLC	2	100.0	100.0	100.0	100.00
5	R99	1K	RLC	2	100.0	100.0	0.0	100.00
6	A5	DISPLAY	SSI/MSI	10	100.0	100.0	100.0	100.00
7	A6	DISPLAY	SSI/MSI	10	100.0	100.0	100.0	100.00
8	A7	DISPLAY	SSI/MSI	10	100.0	100.0	100.0	100.00
9	C1	4.7/10	RLC	2	100.0	100.0	100.0	100.00
10	C2	4.7/10	RLC	2	100.0	100.0	100.0	100.00
11	C3	4.7/10	RLC	2	100.0	100.0	100.0	100.00
12	C4	4.7/10	RLC	2	100.0	100.0	100.0	100.00

Subsequently, it was felt that these problems could be eliminated by utilizing schematic and layout viewers to select components within a functional block and attach a coverage value to each PPVS defect facet to reflect the level of defect coverage provided by specific tests as depicted in figure.

In the example shown, resistor R99 has been highlighted within the schematic viewer and allocated the following PPVS coverage values: Component **[P]**resence = 100%; Component **[P]**olarity = 100%; Component **[V]**alue = 0.0% and **C**omponent **[S]**older = 100%

PPVS fault coverage predictions can either be made for each selected component or by pin. At the component level each PPVS facet is allocated a color code depending upon the level of fault coverage provided by each specific test.



In this example the PPVS icon represents the fault coverage for component A2 in respect to the PPVS criteria, with each pin also declared as having 100% coverage as indicated by the green circles.
The PPVS color coding for device A2 indicates the following declarations:

Presence: 100%
Polarity: 100%
Value: 0%
Solder: 60%

Initially, all selected devices inherit 100% coverage for each of the Presence, Polarity and Value facets. The coverage figure could be graphically updated to reflect customer estimation. The Solder coverage is computed, based on the number of covered pins divided by the total number of device pins.

Declaration by test steps allows:

- A cross-analysis between the test coverage declaration and the functional tester transcript log file will confirm that all the test steps are really implemented within the test program.
- If a test step passes, it identifies the functional area that is free of defects, so if a test step subsequently fails that includes an already tested component; the 'Sherlock algorithm' can identify the probable source of failure.

INHERITANCE METHOD

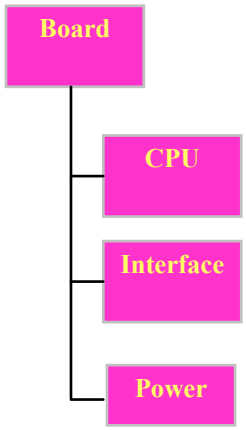
The **Inheritance** method can be utilized to re-use test coverage predictions associated with functional blocks within a design.
This is particular useful within hierarchical design flows that reuse several instances of the same modules/functions, where information can be transferred to multiple instances of the functional block and thus eliminating the need to reproduce the fault coverage predictions for every instance of the design re-use.

This is possible by associating partlist and netlist information with predicted functional test fault coverage figures, so that:

- The module description can either be exported from a CAD module library or extracted from an existing board schematic,
- The functional test coverage details can be supplied manually, from a fault simulator, or by using the TestWay **declaration** method.

During the design analysis phase, the CAD design library will be interrogated for instances of known design modules that are re-used within the board design, so that the corresponding predicted fault coverage can be transferred to the board design.

The module matcher checks if a known module corresponds to a subset of the board.
The module connectivity is compared with the board connectivity and computes a matching percentage between the module and a subset of the board. When the matching percentage equals 100%, the module test coverage is transferred to the board.



The inheritance approach is not limited to functional test coverage only:

- It can be used for sophisticated clusters, combining boundary-scan and emulation, and
- Where emulation is used as a test strategy[7], the inheritance approach can analyze the design hierarchy and pass the coverage variance information to COTS based emulation tools.

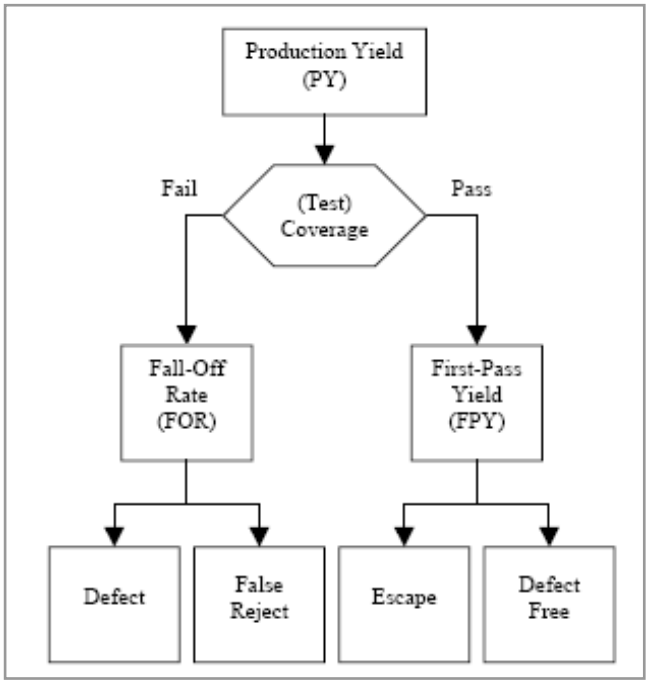
PRODUCTION MODEL

The objective of the production model is to summarize the various facets of the coverage and defect opportunities to provide a limited set of values that will guide the test strategy choice.

- **PY** (Production Yield) represents the probability that a board is good: It is calculated by the accumulation of the defect opportunities on the components (Material, Placement) and the pins (Solder).
- **Test Coverage** is calculated using weighted coverage: According to the level of analysis, it is possible to consider a single test stage or a combination of test stages on the production line.
- **FOR** (Fall-off-Rate) corresponds to the boards that fail test: This group includes real defective boards as well as wrongly rejected boards. These boards will be repaired before integration at the nest stage.

- **FPY** (First Pass Yield) corresponds to the boards that pass test: This group includes good boards, plus bad boards that passed test simply because of insufficient test coverage. The "**escape**" is an effective way to measure the manufacturing quality.
- **ESC** (Escape) corresponds to the escape rate of faulty boards that pass test. This is called 'escape' or 'slip' because they slip through the test process to the customer (final assembly or even into the field). This is the reason for products coming back from the field (end customer) because of process failures, which often result in a 'no fault found (NFF)' scenario due to insufficient test coverage.
  This 'field call rate (FCR)' is not only expensive to repair, but it also damages the brand-name image.

Figure 5: Production Model



COMBINING TEST STRATEGIES

Functional test fault coverage estimations can be used in conjunction with coverage estimations from complementary test strategies such as Automated Optical Inspection (AOI); Automated X-ray Inspection (AXI); In-Circuit test (ICT); Flying Probe test (FPT); Boundary-Scan test (BST) and Functional test (FT) to provide a total fault coverage estimation for the board.

From the complete information database it is possible to determine components that are not covered, but also optimize the overall test strategy to ensure that there is no overlap in the fault coverage provided by tests. This allows the correct balance to be maintained between test time and diagnostic accuracy. The information contained within the fault coverage database can also be utilized to fine tune the test strategy and eliminate any redundant test processes.

It also allows test engineering groups to examine the overall test strategy; so that functional tests can focus on areas where structural test coverage is prohibitive i.e. under RF shielding where physical test access and inspection techniques are not possible.
Alternatively, the combined fault coverage of several boards can be correlated to provide an estimated system level test coverage figure.

CONCLUSIONS

Technological development produces new problems that call for new tools. Test coverage estimation is one of these tools. From design, during production, and in a more general way, through the whole product life cycle, coverage estimation permits the test process to be optimized.
In assessing the results from a combination of test methods it is possible to simulate a variety of test strategies and predict the relative fault coverage[6]. By deploying various testers in the optimum order, at the best time, with controlled levels of redundancies, costs can be reduced and quality levels improved.

The economic challenges are critical; the tools to meet them are available.

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BIOGRAPHIES

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Christophe has over 20 years experience in Board Test.
After working as Electronic Test Manager for the French Navy, he founded the ASTER company in 1993.
As director of the ASTER Product Division, he designed and developed the Testability analyzer, TestWay, widely used by leading OEM and EMS providers.
His research interests are test, Design for Test, and generally speaking Cost Savings from Design to Production.
Christophe is member of BTTAC (formally BTAG).

Peter COLLINS, *Sales & Marketing Manager,* ASTER Technologies
Peter has worked in the test industry for 30 years and is now employed by ASTER Technologies, where he is responsible for global marketing and direct sales of the 'TestWay' Electrical DfT and Fault Coverage Analysis software. Prior to joining ASTER Technologies, Peter worked as a technical marketing consultant with JTAG Technologies, responsible for providing consultancy and training on advanced embedded system level, boundary-scan applications. Peter has authored/co-authored and presented a number of technical papers on board level DfT and boundary-scan related topics at international test conferences, symposiums and workshops worldwide